AN FPGA-BASED ARCHITECTURE FOR THE IN-RUN SELF-CALIBRATION OF MEMS GYROSCOPES

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AN FPGA-BASED ARCHITECTURE FOR THE IN-RUN SELF-CALIBRATION OF MEMS GYROSCOPES

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I dedicate this thesis to my parents Danny and Charlene Wisher

for their love, encouragement, and support

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LIST OF SYMBOLS AND ABBREVIATIONS

MEMS	Microelectromechanical Systems
FPGA	Field-Programmable Gate Array
FOG	Fiber Optic Gyroscope
RLG	Ring Laser Gyroscope
HRG	Hemispherical Resonator Gyroscope
CVG	Coriolis Vibratory Gyroscope
BAW	Bulk Acoustic Wave
TFG	Tuning-fork gyroscope
PCB	Printed circuit board
TIA	Transimpedance amplifier
WLP	Wafer-level packaging
FSR	Full-scale range
ZRO	Zero-rate output
SFD	Squeeze-film damping
TED	Thermoelastic damping
F_C	Coriolis Force
m	Effective mass
v	Particle velocity
Ω_z	Angular rate
x, y	Modal displacement
d_x, d_y	Modal damping
k_x, k_y	Modal stiffness

F_0, F_x, F_y	Actuation force
Q, Q_0, Q_x, Q_y	Quality factor
f, f_0, fx , fy	Resonant frequency
ω, ω_0, ω_x , ω_y	Resonant frequency (angular)
$\Delta\omega$	Mode split
λ	Angular gain
BW_{mech}	Mechanical 3dB bandwidth
V_P	Polarization voltage
v_0	Actuation voltage
F_{elec}	Electrostatic force
U_c	Capacitive energy
A_{el}	Electrode area
g_0	Capacitive gap size
C_0	Static capacitance
$TNE\Omega$	Total noise equivalent rate
$MNE\Omega$	Mechanical noise equivalent rate
$ENE\Omega$	Electrical noise equivalent rate
SF	Scale factor
I_Ω	Rate-induced output current
k_B	Boltzmann constant (1.38×10-23 J/K)
T	Temperature
BW_{meas}	Measurement bandwidth
$I_{n,total}$	Total input-referred noise
$\sigma_\Omega^2(\tau)$	Allan deviation
ARW	Angle random walk

BI	Bias instability
RRW	Rate random walk
d_{xy}, d_{yx}	Damping coupling
k_{xy}, k_{yx}	Stiffness coupling
Q_{xy}, Q_{yx}	Bias error term
ω_{xy}, ω_{yx}	Misalignment term
η	Transduction coefficient
C_{FT}	Feedthrough capacitance
$V_{n,B}$	Quantization noise
V_{ref}	Reference voltage
OSR	Oversampling ratio
DNL	Differential nonlinearity
IL	Insertion loss
AGC	Automatic gain controller
PI	Proportional-integral
VGA	Variable gain amplifier
PLL	Phase-locked loop
LUT	Look-up table
$F_{T,x}$, $F_{T,y}$	Electrostatic tuning force
$V_{T,x}$, $V_{T,y}$	Tuning voltage
V_{Q1}, V_{Q2}	Quadrature compensation voltage
R_F	TIA feedback resistor
V_{CAL}	Calibration voltage for virtual rate stimulus
NI	National Instruments
$FlexRIO$	Flexible reconfigurable I/O

RT	Real-time
SCTL	Single-cycle timed loop
DSP	Digital signal processing
DCM	Digital clock managers
ADC	Analog-to-digital converter
DAC	Digital-to-analog converter
DDS	Direct digital synthesis
CORDIC	Coordinate rotation digital computer
f_{sig}	Sinusoidal signal frequency
f_{clk}	Clock frequency
M	Input word length
FTW	Frequency tuning word
FIR	Finite impulse response
IIR	Infinite impulse response
NCO	Numerically-controlled oscillator
SPI	Serial peripheral interface
$I_{1/f}$	Current flicker noise
g_m	Transconductance
$K_{1/f}$	Process-related flicker noise constant
L	Transistor length
W	Transistor width
C_{ox}	Oxide capacitance
BP-ΣΔ	Bandpass sigma-delta
ΔQ	Difference in quality factor

SUMMARY

Micromachined vibratory gyroscopes have become useful for a wide variety of consumer, industrial, and automotive applications. While they are used effectively in within a certain range of applications, micromachined gyroscopes cannot yet perform to the standards of high-precision inertial systems, the bias and scale factor must exhibit very low drift over long periods of time to prevent false rate measurements. Even with extensive factory calibration, the overall system reliability of MEMS gyroscopes predominantly depends on initial calibration measures which may become inaccurate over time requiring additional calibration. In this thesis, the dual-mode interfacing architecture, developed by the Integrated MEMS group, is implemented on a digital platform with multiple in-run calibration layers to show improvements in overall gyroscope performance.

With the digital implementation of the dual-mode interfacing architecture, in-run calibration of both bias and scale factor is made possible without interfering with the rate readout of the gyroscope. Using this architecture, the angular rate output is inherently bias-free when the insertion losses and frequencies of the modes are matched. For the modal frequencies to remain mode-matched, a mode-split-indicating error signal is extracted from the gyro output and monitored to provide closed-loop automatic mode-matching by adjusting electrostatic tuning voltages to reduce the error signal to zero. Scale factor calibration is implemented by providing an electronic calibration stimulus in the actuation signal that exhibits similar drift over time and temperature as physical scale factor, and since the calibration stimulus being applied to the gyro is known, any changes in this stimulus can be used to compensate for scale factor drift. To show a proof of concept, the

various calibration layers were previously implemented individually using a lock-in amplifier with analog electronics, but by using a digital platform for the implementation of the dual-mode architecture, the calibration layers have been fully integrated. Further details of the digital implementation of this architecture are discussed in this thesis.

Significant improvements are shown through this FPGA-based implementation of the dual-mode architecture compared to the conventional interfacing scheme. The primary components of the experimental setup consist of a Qualtré BAW gyroscope [1], a temperature-controlled rate table, and a National Instruments digital system. The signals are generated and acquired using an adaptor module that attaches to an FPGA board. The FPGA board is secured to a chassis that facilitates communication between the FPGA and a real-time embedded controller to then be sent to a host computer for data analysis. The primary mode by which performance of this system was evaluated was sweeping the temperature and power cycling the system to evaluate drift and repeatability of bias and scale factor. By sweeping temperature from 15-85 °C, the digital dual-mode implementation has demonstrated >20x reduction in bias drift from 40 °/s with conventional operation to 1.8 °/s with dual-mode operation. Using the scale factor calibration scheme, >50x improvement has been demonstrated from 57.5% to 1.1% between conventional and dual-mode. From turn-on to turn-on measurements, bias and scale factor repeatability have also shown improvements of >4x and >10x, respectively, and the future steps of this digital architecture are mentioned to provide a path toward further improvements in the current digital architecture.

CHAPTER 1: INTRODUCTION

Gyroscopes are physical mechanisms used to detect angular rotation. To detect rotation, energy must first be added to the system, and this is achieved through either spinning or vibrating the mass. For decades, rotary gyroscopes have been used in inertial guidance systems for ships, missiles, airplanes, space shuttles, and satellites [2], but the size and complex construction significantly reduce the number of practical applications. For more advanced systems, optical gyroscopes, such as fiber optic gyroscopes (FOGs) and ring laser gyroscopes (RLGs), have been developed by taking advantage of the Sagnac effect, a phenomenon that induces a beat frequency due to a change in path length of two beams when subjected to rotation [3]. Rotary gyros and optical gyros are suitable for many navigation systems, but their applications are limited due to the demands of power, weight, cost, and size.

The most advanced gyroscopes currently in production are the hemispherical resonator gyroscopes (HRGs) that operate based on rotation-induced Coriolis force [4]. HRG systems, developed by Northrop Grumman, have shown comparable performance to that of the RLG, and they can be used on a much wider variety of platforms with greater reliability. Due to their lighter weight and smaller size, they are suitable for many aeronautical applications with less restriction on payload capacity of the vessel, making them ideal for high value missions. The implementation of HRGs has proven to be extremely reliable for spacecraft navigation with over 12 million hours of space missions logged, but to achieve such high performance, sophisticated manufacturing techniques are

used which significantly increases the cost. Some of the various gyroscope structures are illustrated in Figure 1.

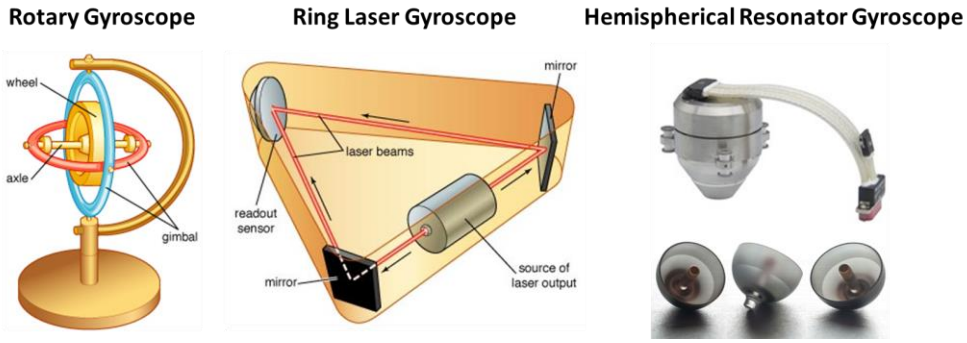


Figure 1 – Illustrations of various gyroscopes with different operating principles.

The great success in the development of Coriolis vibratory gyroscopes (CVGs) has inspired the development of microelectromechanical systems (MEMS) based on similar operation principles. With advancements in fabrication methods for micromachined devices, multiple gyros can be batch fabricated to allow for low cost, and they have become prominent in a wide variety of products such as those in Figure 2. In recent years, promising results have been shown to increase the reliability and precision of micromachined gyroscopes.

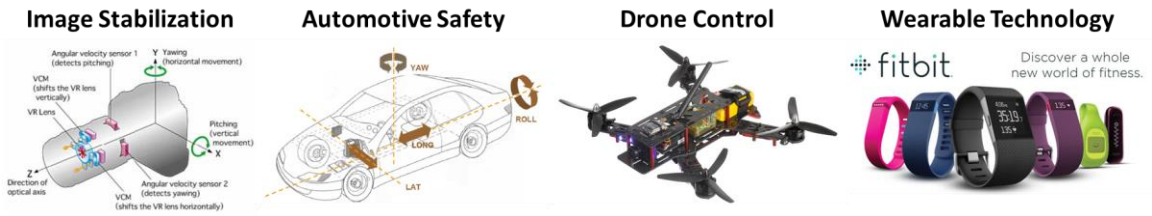


Figure 2 – Various consumer applications for inertial MEMS

Inertial MEMS, such as gyroscopes and accelerometers, are already widely used in smartphones to provide image stabilization and motion detection [5], and they are also

becoming commonplace in the automotive industry for skid and roll detection [6]. Wearable devices and drones have become increasingly popular to consumers [7], [8], and these products require the use of inertial MEMS for motion sensing and platform stabilization. To provide a means for more advanced high-precision applications, various architectures can be used to provide layers of calibration to compensate for the errors in micromachined gyroscopes [9], and the progress of one such architecture is detailed in this thesis.

1.1 Micromachined Coriolis Vibratory Gyroscopes

With great strides being made in the field of MEMS, micromachined gyroscopes have made a considerable impact in such consumer products as smartphones, wearable devices, and automobiles; and as fabrication and interfacing methods improve, the range of applications can increase substantially [10]-[13]. Advanced gyroscope technology can allow for enhanced inertial navigation instrumentation on platforms such as unmanned aerial vehicles (UAVs) where the size and power consumption of high performance gyros may otherwise be a significant limitation for controllability and range.

1.1.1 Principle of Operation

MEMS gyroscopes are micromachined vibratory devices with two resonant modes. One mode is forced into oscillation to provide energy to the system, and when the device is subjected to angular rotation, energy is transferred proportionally to a mode orthogonal to the driven mode and the rotation axis, which can then be sensed to detect angular rate [14], [15]. This phenomenon, called Coriolis force, as illustrated in Figure 3, is a fictitious force that is realized when a point mass is moving within an inertial reference frame being

subjected to rotation. From an observer's point of view in the inertial reference frame, the point mass appears to change its trajectory when rotation is applied, but in reality, the mass motion does not respond to the rotation. With sustained oscillation in the drive mode, this effect induces a vibration in the sense mode which can then be picked off to detect rotation rate, and the resulting Coriolis force can be calculated using equation 1.1 with Coriolis force, mass, velocity, and angular rotation represented as F_C, m, v, and Ω, respectively.

$$\overrightarrow{F_C} = 2m\vec{v} \times \vec{\Omega} \tag{1.1}$$

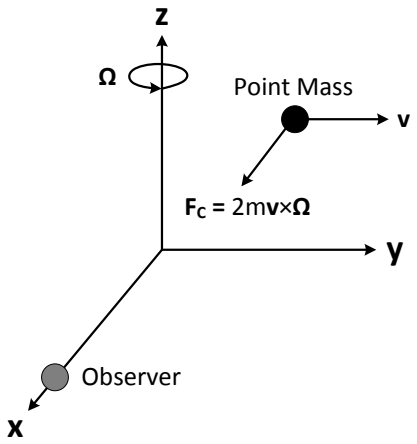


Figure 3 – Illustration showing the Coriolis force of a point mass within an inertial frame of reference.

Gyroscopic modes can be categorized as either non-degenerate or degenerate. The majority of consumer vibratory gyroscopes are designed to have non-degenerate modes, meaning that the two modes do not have a similar shape but do allow for the transfer of energy between the drive mode and sense mode. The most prominent of these designs is the tuning fork gyroscope in which proof masses have support structures that facilitate two-dimensional motion [16]. The proof masses are driven into oscillation, and when subjected

to rotation, energy is transferred to the complementary mode as shown in Figure 4. Gyros with degenerate modes are axisymmetric structures that are usually designed in the shape of a shell, ring, or disk [17]. In these types of structures, the degenerate mode pair constitutes the drive and sense modes shown in Figure 5. The symmetry of these devices allow for a differential readout with near-equal modal parameters.

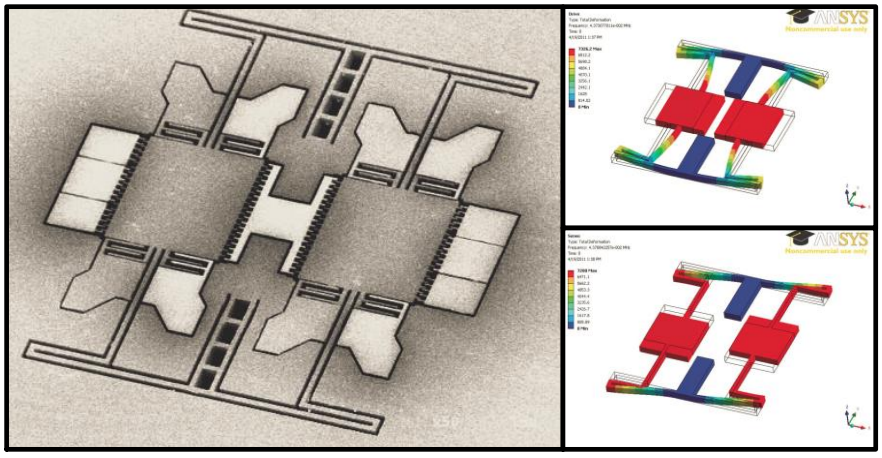


Figure 4 – SEM image of a TFG device along with simulation plots of the gyroscope displacement of the drive and sense modes.

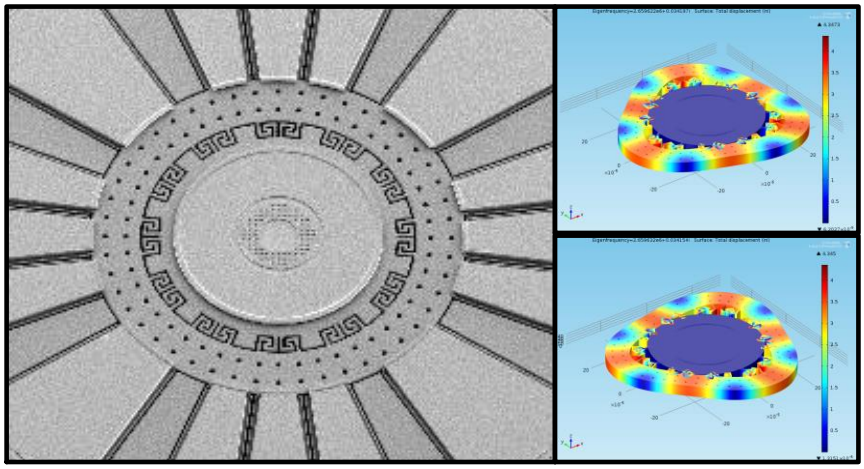


Figure 5 – SEM image of a BAW gyro along with simulation plots of the gyroscope displacement of the drive and sense modes.

An ideal z-axis vibratory gyroscope is mathematically represented as a two degree-of-freedom spring-mass-damper system shown in equation 1.2. The device parameters m, d_i, and k_i represent the effective mass, mode damping, and mode stiffness. External forces applied to each mode are represented as F_i, and angular rate is shown as Ω_z. Angular gain (λ) is a parameter that depends on the geometry and mode shape of the device.

$$\begin{aligned} m\ddot{x} + d_x\dot{x} + k_x x &= f_x(t) - 2m\lambda\Omega_z\dot{y} \\ m\ddot{y} + d_y\dot{y} + k_y y &= f_y(t) + 2m\lambda\Omega_z\dot{x} \end{aligned} \tag{1.2}$$

The conventional representation of an ideal gyro system is given by the system of equations shown in equation 1.3, where the device parameters are reinterpreted to include quality factor (Q_i) and natural frequency (ω_i) according to the following parametric identities: $d_i/m=\omega_i/Q_i$ and $ki/m=\omega_i^2$.

$$\begin{aligned} \ddot{x} + \frac{\omega_x}{Q_x}\dot{x} + {\omega_x}^2 x &= \frac{|F_x|\cos(\omega_x t)}{m} - 2\lambda\Omega_z\dot{y} \\ \ddot{y} + \frac{\omega_y}{Q_y}\dot{y} + {\omega_y}^2 y &= 2\lambda\Omega_z\dot{x} \end{aligned} \tag{1.3}$$

In this particular mode of operation, a sinusoidal actuation force is applied along the *x*-mode (drive mode) to facilitate angular rate sensing in the *y*-mode (sense mode). To simplify analysis, this system is often represented in the frequency domain with the Coriolis-induced rate signal influence on the drive mode considered to be negligible due to the large drive force as shown in equations 1.4 and 1.5.

$$\begin{bmatrix} -\omega^2 + j\omega\frac{\omega_x}{Q_x} + {\omega_x}^2 & 0 \\ -j\omega \cdot 2\lambda\Omega_z & -\omega^2 + j\omega\frac{\omega_y}{Q_y} + {\omega_y}^2 \end{bmatrix} \cdot \begin{bmatrix} X(j\omega) \\ \\ Y(j\omega) \end{bmatrix} = \begin{bmatrix} \frac{F_x}{m} \\ \\ 0 \end{bmatrix} \tag{1.4}$$

It can then be assumed that the sinusoidal drive force frequency (ω) is equal to the drive mode frequency (ω_x) to yield the following time-domain displacement result of equation 1.6.

$$X(j\omega) = \frac{F_x/m}{{\omega_x}^2 - \omega^2 + j\omega\frac{\omega_x}{Q_x}} \tag{1.5}$$

$$Y(j\omega) = \frac{j\omega \cdot 2\lambda\Omega_z}{\left({\omega_y}^2 - \omega^2 + j\omega\frac{\omega_y}{Q_y}\right) \cdot \left({\omega_x}^2 - \omega^2 + j\omega\frac{\omega_x}{Q_x}\right)}\frac{F_x}{m}$$

$$x(t) = \frac{|F_x|Q_x}{m{\omega_x}^2}\sin(\omega_x t)$$

$$y(t) = \frac{2\lambda\Omega_z Q_x|F_x|}{m\omega_x\sqrt{\left({\omega_y}^2 - {\omega_x}^2\right)^2 + \left(\frac{\omega_x\omega_y}{Q_y}\right)^2}}\cos(\omega_x - \varphi), \quad \varphi = \tan^{-1}\frac{\omega_x\omega_y/Q_y}{{\omega_y}^2 - {\omega_x}^2} \tag{1.6}$$

The mode frequency split is considered when interfacing the gyroscope outputs. Mode-matched operation is the condition under which the resonant frequencies of each mode are equal, and mode-split operation is realized when the difference between the resonant frequencies ($\Delta\omega = \omega_y - \omega_x$) is greater than the 3dB bandwidth of the sense mode response ($BW_{mech,y}$), defined as ω_y/Q_y. Under mode-matched condition ($\Delta\omega = 0$), the equations for displacement can be simplified as:

$$x(t) = \frac{|F_x|Q_x}{m{\omega_x}^2}\sin(\omega_x t)$$
$$y(t) = \frac{2\lambda\Omega_z Q_x Q_y |F_x|}{m{\omega_x}^3}\sin(\omega_x t) \tag{1.7}$$

Mode-split condition, the design methodology commonly used in consumer rate-grade gyroscopes, is simplified to yield the following equations for mode displacement based on the assumption that the resonant modes are significantly larger than the mode split:

$$x(t) = \frac{|F_x|Q_x}{m{\omega_x}^2}\sin(\omega_x t)$$
$$y(t) = \frac{2\lambda\Omega_z Q_x |F_x|}{m{\omega_x}^2\sqrt{(2\Delta\omega)^2 + \left(\omega_y/Q_y\right)^2}}\cos\left(\omega_x t - \tan^{-1}\frac{\omega_y/Q_y}{2\Delta\omega}\right) \tag{1.8}$$

While mode-split operation allows for relatively low drift in the rate readout over temperature, its effectiveness is heavily dependent on the gyroscope design to ensure that a suitable signal-to-noise ratio is achieved with large proof masses and transduction area. Mode-matched operation offers the benefit of optimal sensitivity from angular rate, but deviations from mode-matched condition across time and temperature induces drift in the rate output.

1.1.2 Transduction of Capacitive MEMS Gyroscopes

In the case of Coriolis vibratory gyroscopes, capacitive transduction is a widely-used method to force the device into oscillation and to pick off the output signals. To provide a means for optimal transduction with sufficient linearity, parallel-plate transducers are used to interface the gyroscope as shown in Figure 6.

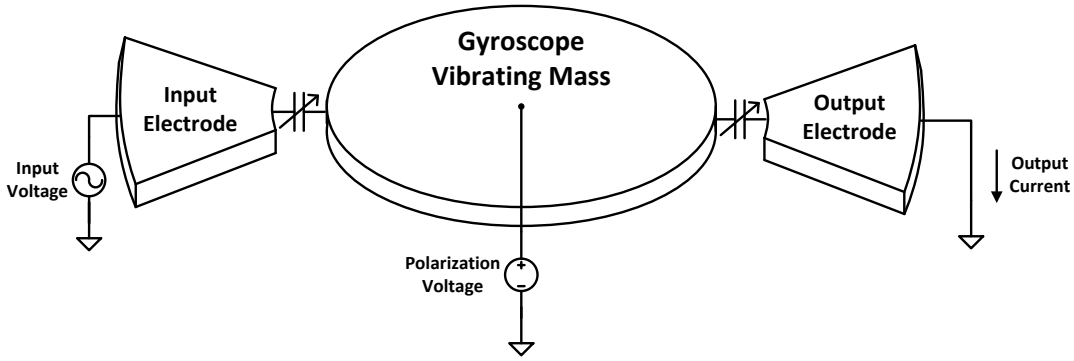


Figure 6 – Illustration showing the application of polarization voltages along with drive and sense outputs.

1.1.2.1 Drive Mode Actuation Force

To provide a sinusoidal electrostatic force to the drive mode, a DC polarization voltage (V_P) is applied to the vibrating body of the gyroscope while an AC voltage (v_0) is applied to an electrode that is aligned to the drive mode. To investigate this effect, the known relationship between electrostatic force (F_{elec}) and capacitive energy (U_c) with respect to displacement (x) is utilized, and the parameters of the capacitive transducer are electrode area (A_{el}) and capacitive gap size (g_0) as shown in the equation below:

$$F_{elec} = -\frac{\partial W_{cap}}{\partial x} = -\frac{\partial}{\partial x}\left[\frac{1}{2}\cdot\frac{\varepsilon_0 A_{el}}{x-g_0}\cdot(V_P+v_0)^2\right] \\ = \frac{1}{2}\cdot\frac{\varepsilon_0 A_{el}}{(x-g_0)^2}\cdot\left({V_P}^2+2V_P v_0+{v_0}^2\right) \quad (1.9)$$

To simplify equation 1.9, it can be assumed that V_P and g_0 are substantially larger than v_{AC} and x, respectively. This assumption allows $1/(x/g_0 - 1)^2$ to be approximated to $1 + 2x/g_0$. The static capacitance term, C_0, is also used to replace $\varepsilon_0 A_{el}/g_0$ to yield the following relationship containing only the AC terms:

$$F_{elec,AC} = \frac{C_0 V_P}{g_0} \cdot v_0 \cos(\omega t) + \frac{C_0 {V_P}^2}{{g_0}^2} x \tag{1.10}$$

The resonant mode of the gyro is driven into oscillation with an AC voltage, and the polarization voltage also results in an amplitude-modulated force that alters the effective frequency of the resonant modes, and the electrostatic force of equation 1.10 is combined with equation 1.3 to yield the following relationship:

$$\begin{aligned} \ddot{x} + \frac{\omega_x}{Q_x}\dot{x} + \left({\omega_x}^2 - \frac{1}{m} \cdot \frac{C_0 {V_P}^2}{{g_0}^2}\right) x &= \frac{1}{m} \cdot \frac{C_0 V_P}{g_0} \cdot v_0 \cos(\omega t) \\ \ddot{y} + \frac{\omega_y}{Q_y}\dot{y} + \left({\omega_y}^2 - \frac{1}{m} \cdot \frac{C_0 {V_P}^2}{{g_0}^2}\right) y &= 2\lambda \Omega_z \dot{x} \end{aligned} \tag{1.11}$$

1.1.2.2 Sense Mode Output Pick-off

The motion of the vibrating structure can be sensed through the current being outputted to an electrode. The relationship by which current is sensed from mode velocity is shown below:

$$i(t) = C\frac{\partial v}{\partial t} + V\frac{\partial C}{\partial t} \approx V\frac{\partial C}{\partial t} = V\frac{\partial C}{\partial x}\frac{\partial x}{\partial t} \approx \frac{C_0 V_P}{g_0} \cdot \frac{\partial x}{\partial t} \tag{1.12}$$

To translate this relationship to be used with the gyro equations, equation 1.12 can be rewritten as:

$$I(j\omega) = \frac{C_0 V_P}{g_0} \cdot j\omega X(j\omega) \rightarrow \frac{I(j\omega)}{X(j\omega)} = j\omega \cdot \frac{C_0 V_P}{g_0} \tag{1.13}$$

While using a switching capacitor circuit is suitable for many low-frequency tuning-fork gyroscope designs, current sensing is far more suitable for high-frequency gyroscopes due to the velocity output, which is directly proportional to frequency.

1.2 Gyroscope Performance Specifications

For classification of gyroscope performance, the target specifications are given in [18] to evaluate whether a gyro is rate-grate, tactical-grade, or navigation-grade as shown in Table 1. While most consumer MEMS gyroscopes are rate-grade, great strides have been made to achieve tactical grade, and there is great interest in pushing the boundaries of MEMS technology to eventually achieve navigation-grade performance allowing for a more extensive range of applications.

Table 1 – Required specifications for various classes of gyroscopes

Parameter	Unit	Rate Grade	Tactical Grade	Inertial Grade
Angle Random Walk	°/√h	>0.5	0.5-0.05	<0.001
Bias Drift	°/h	10-1000	0.1-10	<0.01
Scale Factor Accuracy	%	0.1-1	0.01-0.1	<0.001
Full Scale Range	°/s	50-1000	>500	>400
Max. Shock in 1 ms	g	10^3	10^3-10^4	10^3
Bandwidth	Hz	>70	~100	~100

1.2.1 Resolution

Vibratory gyroscope resolution is defined as the minimum detectable angular rate in the output. Detailed in this section are the key measures to be taken into account to achieve a low-noise rate output. The mechanical parameters of the gyro design and the noise of the interface electronics both contribute to the bias and scale factor drift in the gyro output. The mechanical noise equivalent rate and electrical noise equivalent rate are represented as MNE and ENE, respectively, and the noise powers can be added as shown below to define the total noise equivalent rate:

$$TNE\Omega = \sqrt{MNE\Omega^2 + ENE\Omega^2} \tag{1.14}$$

1.2.1.1 Scale Factor

The scale factor specification, also defined as angular rate sensitivity, is defined as the electrical output response due to the Coriolis force induced by angular rate. The mechanical parameters of the gyroscope device determine the scale factor, and it is often represented as either pA/°/s or mV/°/s. Combining the mode-matched gyroscope relationship of equation 1.5 with the transfer function for output current shown in equation 1.14, the displacement of the sense mode can be translated into an amplitude-modulated current output (I_Ω) related to rotation rate as shown in the following equation:

$$\left|\frac{I_\Omega}{\Omega_z}\right| = \frac{2\lambda V_P Q_y C_0 |x|}{g_0} \tag{1.15}$$

1.2.1.2 Mechanical and Electrical Noise Equivalent Rate

Mechanical noise equivalent rotation is generated by the Brownian motion in the mass of the gyroscope. This motion can be modelled as an input force to the sense mode, and the resulting noise for mode-matched gyros can be translated to rate as shown in the following equation:

$$MNE\Omega = \frac{1}{\lambda|x|}\sqrt{\frac{k_B T}{m\omega_y Q_y}}\sqrt{BW_{meas}} \tag{1.16}$$

In this relationship, k_B and T represent the Boltzmann constant (1.38×10-23 J/K) and the ambient temperature, respectively, and BW_{meas}, in this case, is the measurement bandwidth of the system.

Another key metric to consider is the noise induced by the electronics as it is perceived at the interface between the electrode and sense circuit. Since mode-matched operation is the optimal case for a large scale factor, it is ideal for a minimal *ENEΩ*. In this case, the electronic noise is represented as the total input-referred noise ($I_{n,total}$), and it can be translated to angular rate as shown below:

$$ENE\Omega = \frac{g_0}{2\lambda V_P C_0 Q_y|x|} I_{n,total}\sqrt{BW_{meas}} \tag{1.17}$$

1.2.2 Allan Variance Analysis

Allan variance, also known as Allan deviation, is a time-domain measurement method originally developed to analyze the long-term frequency stability of oscillators [19]. This method is also useful to measure the bias stability of sensors and to differentiate

stochastic noise processes from a device's sensitivity to external, deterministic factors. To determine gyroscope performance for inertial navigation accuracy, this method is often used to measure of long-term bias drift. For the purpose of gyroscope measurements, the following equation can be applied to calculate Allan deviation in terms of angular rate [20]-[22]:

$$\sigma_{\Omega}{}^{2}(\tau) = \frac{1}{2(N-1)} \sum_{j=1}^{N-1} (\Omega_{k+1} - \Omega_{k})^{2} \tag{1.18}$$

This equation represents the Allan deviation ($\sigma_{\Omega}{}^{2}(\tau)$) processed with N samples of angular rate (Ω_j) data.

By plotting root Allan variance ($\sigma_{\Omega}(\tau)$) in °/h, the time-domain noise and drift contributors can be determined by the log-log slope of a line fit to a given plot section. Figure 7 is an illustration of an Allan variance plot with the most relevant noise and drift terms for gyroscopes. Quantization noise, angle random walk, bias instability, rate random walk, and rate ramp are shown in this plot with their associated slopes. The combined effect of all noise contributors is defined as the addition of the Allan deviations as shown below where the contributors designated as $\sigma_{Quant}{}^{2}(\tau)$, $\sigma_{ARW}{}^{2}(\tau)$, and $\sigma_{BI}{}^{2}(\tau)$ represent quantization noise, angle random walk, and bias instability respectively.

$$\sigma_{total,\Omega}{}^{2}(\tau) = \sigma_{Quant}{}^{2}(\tau) + \sigma_{ARW}{}^{2}(\tau) + \sigma_{BI}{}^{2}(\tau) + \cdots \tag{1.19}$$

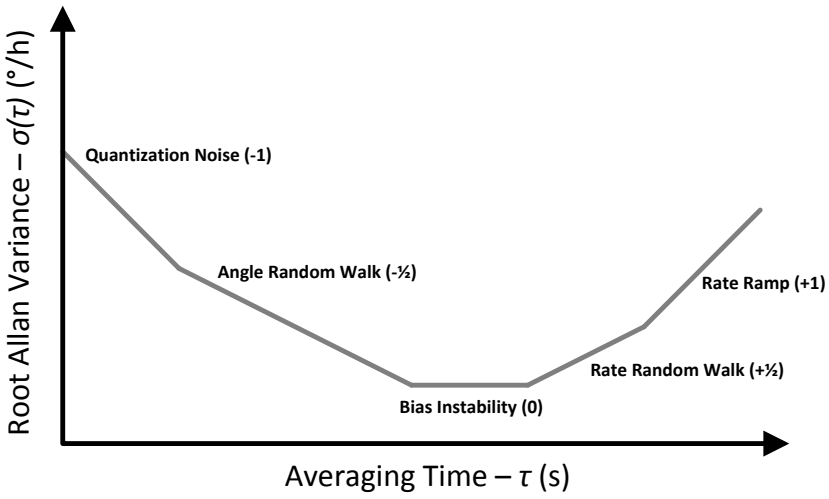


Figure 7 – Example plot for root Allan variance analysis showing the various noise classifications.

1.2.2.1 Quantization Noise

The quantization noise of a gyroscope system is represented with a slope of -1 on a log-log root Allan variance plot. This type of noise is primarily induced by the digital components of the readout electronics, and in terms of root Allan variance, the quantization noise in terms of angular rate can be represented as:

$$\sigma_{Quant}(\tau) = \frac{\sqrt{3}Q}{\tau} \tag{1.20}$$

1.2.2.2 Angle Random Walk

Angle random walk (ARW), represented with a -1/2 slope on a root Allan variance plot, is random noise with a constant spectral density. This white noise is sourced from the thermal noise of system components, and it is represented as:

$$\sigma_{ARW}(\tau) = \frac{N}{\sqrt{\tau}} \tag{1.21}$$

ARW is easily quantified as N in equation 1.21 by measuring the point on the slope where $\tau = 1\ s$. The unit of this measured value is °/h/√Hz, and it is often divided by 60 to be represented with the unit of °/√h.

1.2.2.3 Bias Instability

Bias instability is recognized as the zero-slope section of an Allan variance plot where there is no longer a reduction in drift with averaging. The value of bias instability is an indication of how stable the gyroscope bias will be over a specified time period making it one of the most important specifications for a high-performance gyroscope. Typically represented with the unit of °/h, the contribution of this effect is the electronic flicker noise that causes bias fluctuations in the rate output. In the case of flicker noise, the noise has a 1/f trend; therefore, when the averaging time increases and the flicker noise dominates, the low frequency noise prevents further reduction in Allan deviation.

1.2.2.4 Rate Random Walk/Rate Ramp

Rate random walk (RRW) is a low-frequency phenomenon whose influence is primarily unknown. While the $1/f^2$ close-in phase noise of the drive-loop signals may induce this type of low-frequency drift behavior, RRW will not be the dominating low-frequency term in the gyros presented in this thesis. Rate ramp is the more dominant source of low-frequency drift as it is related to slow monotonic changes over a long period of time. In the case of rate ramp of MEMS gyroscopes, bias can be sensitive to slow environmental

changes such as temperature and pressure. To prevent pressure changes, it is beneficial to wafer-level package (WLP) devices to provide a stable, low-pressure environment, and to reduce bias sensitivity to temperature, layers of compensation and calibration can be added.

1.2.3 Bandwidth

The mechanical bandwidth of a mode-matched gyroscope is defined by the resonant frequency (f_0) divided by the quality factor (Q) of a particular device. Bandwidth defines the full-scale range of the angular rate output, making a large bandwidth a highly favorable specification since, in terms of bandwidth, 1 Hz = 360 °/s. In mode-matched devices, high-Q gyroscopes are able to provide favorable noise performance and scale factor, but with low-frequency resonant modes, the bandwidth of these devices is limited. High-frequency mode-matched BAW gyroscopes provide a means for high-performance angular rate measurements with an enhanced range of applications. Many of its low-frequency counterparts have shown exceptional drift performance, but they are unable to be used for many practical applications as they have a limited full-scale range (FSR) as defined by the mechanical half-bandwidth converted from hertz to °/s:

$$FSR\ [^\circ/s] = 360 \cdot \frac{f_0}{2Q} \tag{1.22}$$

An increased bandwidth also allows for a fast transient response to angular rate stimuli providing high-speed feedback for control systems.

1.2.4 Shock and Vibration Sensitivity

Due to the increased stiffness, BAW gyroscopes also improve gyroscope performance when subjected to shock and vibration [23]. When subjected to either stimulus, it is the resonant frequency of translational modes that is important to consider as these modes are the most responsive modes to linear acceleration. Since the translational mode frequencies are defined by the support structure similarly to the gyroscope modes in TFG designs, the rate output becomes vulnerable to shock and vibration. In contrast to TFG structures, the gyroscopic modes of BAW devices are defined primarily by the radial dimensions while the translational modes are defined by the support structure making the mode pairs intrinsically far apart. It is also important to consider the frequency response of the translational modes when subjected to external vibration. TFGs, which typically have resonant frequencies of on the order of 1-10 kHz, are vulnerable to acoustic vibrations which can induce error in the rate output.

1.3 Gyroscope Error Sources

Physical non-idealities of MEMS vibratory gyroscopes can induce drift in the rate output to deteriorate performance. While the drift sources, discussed in this section, can be compensated in some cases, drift over time and temperature can still effect these parameters to result in long-term instability in the rate output. Interface electronics can also induce drift with performance determined by such specifications as analog reference drift, amplifier gain drift, and flicker noise. In the following subsections, a non-ideal gyroscope model is examined, and the errors indicated by this model are discussed.

1.3.1 Non-ideal Gyroscope Model

Fabrication imperfections of MEMS gyroscopes can be modeled by adding terms in the gyro equations that represent sources of error in the angular rate output [24], [25]. The effects of anisodamping and anisoelasticity are considered in the equation below:

$$\begin{aligned} m\ddot{x} + d_x\dot{x} + k_x x + d_{yx}\dot{y} + k_{yx}y &= f_x(t) - 2m\lambda\Omega_z\dot{y} \\ m\ddot{y} + d_y\dot{y} + k_y y + d_{xy}\dot{x} + k_{xy}x &= f_y(t) + 2m\lambda\Omega_z\dot{x} \end{aligned} \tag{1.23}$$

Damping coupling (d_{yx} and d_{xy}) and stiffness coupling (k_{yx} and k_{xy}) are introduced in this equation, and in axisymmetric devices, it can be assumed that $d_{yx} = d_{xy}$ and $k_{yx} = k_{xy}$. Equation 1.23 can also be simplified by converting by representing the damping and stiffness in terms of quality factor and resonant frequency, and in conventional gyro operation, $f_x(t)$ and $f_y(t)$ are $F_x\cos(\omega t)$ and 0, respectively:

$$\begin{aligned} \ddot{x} + \frac{\omega_x}{Q_x}\dot{x} + {\omega_x}^2 x + \frac{\omega_{xy}}{Q_{xy}}\dot{y} + {\omega_{xy}}^2 y &= \frac{F_x}{m}\cos(\omega t) - 2\lambda\Omega_z\dot{y} \\ \ddot{y} + \frac{\omega_y}{Q_y}\dot{y} + {\omega_y}^2 y + \frac{\omega_{xy}}{Q_{xy}}\dot{x} + {\omega_{xy}}^2 x &= 2\lambda\Omega_z\dot{x} \end{aligned} \tag{1.24}$$

With a more extensive gyro model, the system of equations can be simplified by translating it to the frequency domain:

$$\begin{bmatrix} {\omega_x}^2 - \omega^2 + j\omega\frac{\omega_x}{Q_x} & {\omega_{xy}}^2 + j\omega\left(\frac{\omega_{xy}}{Q_{xy}} + 2\lambda\Omega_z\right) \\ {\omega_{xy}}^2 + j\omega\left(\frac{\omega_{xy}}{Q_{xy}} - 2\lambda\Omega_z\right) & {\omega_y}^2 - \omega^2 + j\omega\frac{\omega_y}{Q_y} \end{bmatrix} \cdot \begin{bmatrix} X(j\omega) \\ \\ Y(j\omega) \end{bmatrix} = \begin{bmatrix} \frac{F_x}{m} \\ \\ 0 \end{bmatrix} \tag{1.25}$$

Solving for the Coriolis-induced modal displacement, assuming mode-matched condition ($\omega_x = \omega_y = \omega_0$), yields the following equation:

$$Y(j\omega_0) = \frac{\frac{|F_x|Q_xQ_y}{m{\omega_0}^3}\left[\frac{{\omega_{xy}}^2}{\omega_0} + j\left(\frac{\omega_{xy}}{Q_{xy}} - 2\lambda\Omega_z\right)\right]}{1 + \frac{Q_xQ_y}{{\omega_0}^2}\left[\left(\frac{{\omega_{xy}}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2\right]} \tag{1.26}$$

1.3.2 Bias and Scale Factor Drift

Most sources of bias and scale factor drift can be attributed to mechanical variations with time and temperature. The undesirable coupling between modes can cause drift in the rate output with imperfect demodulation of the signals, and drift in quality factor and resonant frequency also contribute to the output drift.

1.3.2.1 Stiffness and Damping Coupling

In theory, angular rate and stiffness coupling terms can be perfectly decoupled through I/Q demodulation. Although these stiffness terms, often called quadrature, can be significantly reduced through electrostatic compensation, they are still significant contributors to the output magnitude. Therefore, slight variations in the phase of the demodulation signals over time and temperature can induce quadrature leakage into the rate output to deteriorate bias stability. This false rate, induced by the quadrature signal, contributes to what is referred to as the zero-rate output (ZRO). Another contributor to ZRO is the damping coupling terms that have a common phase characteristic to angular rate and are also prone to drift over time and temperature.

1.3.2.2 Quality Factor

Changes in quality factor across time and temperature induce variations in both bias and scale factor. Quality factor is defined as stored energy versus dissipated energy in the gyroscopic modes [26]. In most gyros, the total quality factor (Q_{TOTAL}) is determined by the quality factor contributions of squeeze-film damping (Q_{SFD}), anchor loss (Q_{ANCHOR}), surface loss ($Q_{SURFACE}$), thermoelastic damping (Q_{TED}), and Akheiser loss (Q_{AKE}) as shown by the equation below:

$$\frac{1}{Q_{TOTAL}} = \frac{1}{Q_{SFD}} + \frac{1}{Q_{ANCHOR}} + \frac{1}{Q_{SURFACE}} + \frac{1}{Q_{TED}} + \frac{1}{Q_{AKE}} \tag{1.27}$$

Squeeze-film damping comes from the air gaps between the vibrating body and the electrodes as well as the pressure level of the environment. Wafer-level packaging provides a stable, low-pressure environment for the device to mitigate the damping effect. By designing the mechanical supports in such a way that the vibrating body is decoupled from the substrate, the elastic energy being dissipated through the supports can be significantly reduced. This design methodology prevents the anchor loss from being the limiting term for the total quality factor. In substrate-decoupled, wafer-level packaged gyros, the Q_{TOTAL} in the device shown in this thesis is primarily limited by Q_{SFD} and Q_{TED}, but it is ultimately limited by Q_{AKE}, the intrinsic loss of the material. Scattering losses in devices with rough surfaces can reduce the $Q_{SURFACE}$, but ultimately, the surface loss is not a limitation when advanced fabrication processes are used to provide smooth surfaces. With the main contributors known, the Q_{TOTAL} behaves predictably across temperature.

1.3.2.3 Capacitive Transduction

Bias drift can also arise from variations in the transduction coefficient (η). The transduction coefficient is the term that describes the relationship between mode displacement and electrical signals. Equation 1.13 shows the transduction relationship between mode displacement and output current, and using η, this equation can be rewritten as:

$$\eta = \frac{C_0 V_P}{g_0} \rightarrow \frac{I(j\omega)}{X(j\omega)} = j\omega\eta \tag{1.28}$$

Change in η is mostly due to thermal expansion in the vibrating body that causes small variations in the capacitive gap.

1.3.2.4 Capacitive Feedthrough

Feedthrough capacitance (C_{FT}) appears in capacitive MEMS gyroscopes due to the parasitic capacitances between the vibrating structure, electrodes, substrate, device traces, and PCB traces, and it can be modeled as a series capacitor between each signal port. Since capacitance is temperature dependent, it can induce error in the phase response of the gyro, and a low-drift phase response is paramount for stable closed-loop analysis. With careful design consideration in both the device and circuit layout to provide symmetric signal paths, feedthrough capacitance can become negligible. With the common-mode nature of feedthrough capacitance and with a careful layout design, each signal path typically exhibits similar feedthrough that is mostly cancelled when subtracting the differential signals. However, if there is residual feedthrough capacitance or if differential signals are not available from the gyro, it is possible to implement a feedthrough cancellation circuit as shown in Figure 8:

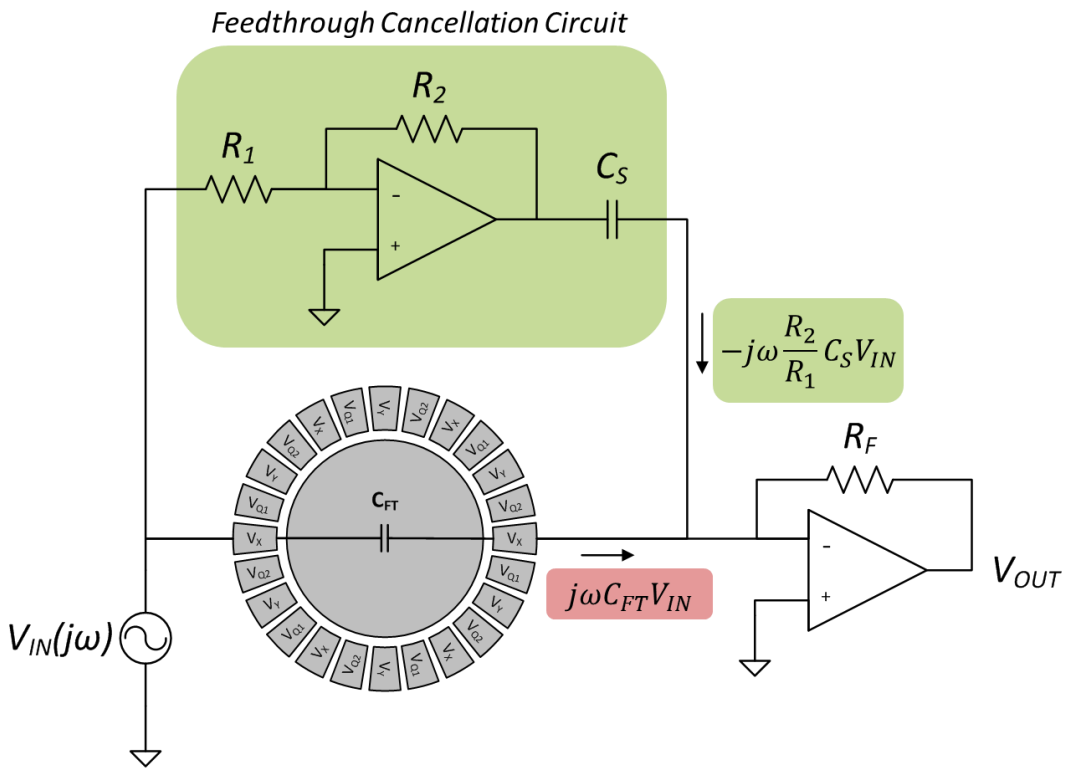


Figure 8 – Diagram showing cancellation circuit for feedthrough capacitance implemented in parallel to a MEMS gyroscope.

1.4 Motivation

The ultimate goal is for micromachined gyroscopes to demonstrate high-grade performance on a small platform with low power consumption. Since MEMS gyroscopes are prone to drift due to the mechanical nonidealities, extensive factory calibration and packaging is necessary to achieve tactical-grade performance which significantly increases the cost [27], [28]. To make high-grade gyroscopes available for a wider range of applications, it is desirable to reduce or eliminate the factory calibration steps while still showing good performance. By modifying the gyro readout method, techniques have been developed to compensate for nonidealities through use of the alternative architectures. Ultimately, the goal is to enhance the gyroscope interfacing architecture to convert a low-

cost, batch-fabricated gyro, which would usually perform poorly under conventional operation, to a high-performance gyro. While some self-calibrated gyro architectures improve performance in certain areas, there are often trade-offs that reduce their practicality. Since changes in environmental conditions can induce drift in the gyroscope output it is desirable to provide a means for in-run calibration in a way that the calibration layers that do not interfere with angular rate readout thus enabling superior gyro performance with no new limitations, and the architecture presented in this thesis seeks to achieve just that.

An excess of analog electronics can present additional drift sources making them unsuitable for the full implementation of the dual-mode architecture; therefore, the most appropriate platform for in-run gyro calibration is through use of digital electronics with minimal analog components. With a digital interfacing architecture, a new level of reconfigurability is available for a higher level of versatility compared to the analog counterpart, and it allows for in-field firmware updates. The system described in this thesis provides inherent bias cancellation and automatic mode-matching to reduce bias drift, and it also provides a means for scale factor calibration.

The work in this thesis presents, for the first time, a full implementation of an in-run self-calibrated gyro architecture is demonstrated on an FPGA-based digital platform to be compatible with high-frequency BAW gyroscopes, and measurements show >20x improvement in bias drift and >40x improvement in scale factor drift across temperature (15-85 °C) compared to the conventional interfacing scheme. Bias and scale factor repeatability also show improvement by >4x and >10x, respectively, and with the next generation of the digital architecture, the performance will be further enhanced.

1.5 Thesis Organization

The remaining chapters are organized as follows. Chapter 2 discusses the basic building blocks for low-noise gyro interfacing systems. Open-loop and closed-loop characterization methods are also introduced, and electrostatic compensation for misalignment and mismatch of resonant modes is also shown.

Chapter 3 shows the implementation schemes for the conventional architecture and the dual-mode architecture, and comparisons are drawn between the two architectures. The various calibration layers of the dual-mode architecture are also introduced.

Chapter 4 gives the details of the digital architecture. The hardware used for the implementation of the architecture is mentioned along with the specifications. The signal chain details are also included from the synthesis of the waveforms to the signal demodulation and filtering. The phase-locked loop for closed-loop gyro operation is discussed along with its individual building blocks, and finally, the implementation of automatic mode-matching and scale factor calibration are shown.

Chapter 5 gives the evaluation of system performance by showing the measurements taken with the experimental setup. The methods by which the data was measured are mentioned, and the results are shown for long-term bias instability, temperature sweep measurements, and turn-on to turn-on repeatability measurements.

Chapter 6 discusses the remaining error sources that contribute to the performance setbacks of the digital system. The noise induced from the data converters are mentioned, and it is shown that certain measurement capabilities are being limited as a result. The

shortcomings of the current scale factor calibration scheme are given along with ideas for future improvements. Ideas are also presented for bias instability reduction, improved scale factor measurement methods, and insertion loss mismatch compensation, and the vision for the final stage of the project is also briefly discussed.

CHAPTER 2: GYROSCOPE OPERATION PRINCIPLES

For full gyroscope characterization and operation, it is important to know various techniques for device measurements. In practical MEMS gyroscope systems, analog circuits are used for buffering the actuation signals and amplifying the pick-off signals, and depending on whether a digital or analog interface architecture is used, additional analog circuitry may be needed. Open-loop measurements can then be taken to characterize the mechanical parameters of the device to prepare for a closed-loop implementation. Closed-loop is the mode of operation that enables the angular rate readout of the gyro.

2.1 Low-Noise Electronics

For low-noise, low-drift applications, care must be taken to provide a precise means for amplification of the pick-off gyro signals. While some minimal analog electronics are always required, in a digital interface architecture, certain benefits and limitations in noise and drift are observed.

2.1.1 Analog Electronics

The first step for a low-noise electronic design is the pick-off method for gyro signal amplification. Capacitive transducers typically use switching-capacitor amplifiers, continuous-time charge integrators, and transimpedance amplifiers (TIAs). While switching-capacitor amplifiers and continuous-time charge integrators are suitable choices for many low-noise, low-frequency analog front-ends, TIAs are most suitable for high-frequency gyroscopes [29]. By sensing and amplifying the current signals rather than capacitance, modal velocity is sensed rather than displacement to counter the level of signal attenuation from the inverse relationship of Coriolis coupling with resonant frequency.

In addition to pick-off circuits, an all-analog drive loop architecture, described in Section 2.3, can be implemented for self-sustained closed-loop operation. This architecture requires precise, low-drift phase shifters to lock in to the drive mode. If not carefully designed with high-performance components, the phase shift can drift over time and temperature to make the operating frequency deviate from the resonant mode and induce drift in bias and scale factor. This type of architecture requires analog mixers for I/Q signal demodulation which complicates implementation with discrete components and adds noise to the system. To increase system reliability and reduce the number of components that are prone to drift, it is beneficial to implement gyro functions in the digital domain.

2.1.2 Digital Electronics

By implementing the interface architecture in the digital domain, the pick-off TIAs are still used, but the sources of noise and drift are reduced to the reference error, data converter error, clock jitter, and data truncation error. Quantization noise results from the error between the digitized signal and the analog signal of the data converters due to the finite nature of digital signals. The overall quantization noise can also be reduced by increasing the oversampling ratio (OSR) and resolution bits (N), and the quantization noise power equation is shown below [30]:

$$V_{n,B}{}^2 = \frac{V_{ref}{}^2}{12 \cdot 2^{2N}} \cdot \frac{1}{OSR} \tag{2.2}$$

$V_{n,B}{}^2$ and V_{ref} represent the noise power and the reference voltage, respectively. The OSR represents how many times higher the sampling rate is than the minimum sampling rate.

Sample jitter and harmonic distortion also contribute to the noise power [31]. Jitter causes voltage error in the digitized signal due to instantaneous sampling time error. With a large OSR and stable clock reference, the jitter noise can be minimized to not limit the

overall noise performance of the system. Harmonic distortion is primarily attributed to the physical mismatches in the data converter layout that gives a non-zero differential nonlinearity (DNL), measured as deviation from the ideal digitized signal in least significant bits [32]. The majority of noise from spectral impurity can be filtered; however, it is beneficial to increase the OSR to minimize the overall distortion and reduce the required attenuation of harmonics in the later steps of the signal chain.

2.2 Open-Loop Gyroscope Characterization

One important measurement method is that of open-loop characterization. This is accomplished by sweeping the input frequency to visualize the magnitude and phase of the gyro transfer function. Various mechanical characteristics of gyroscopes can be analyzed using open-loop measurements such as the resonant frequency, frequency split, quality factor, and insertion loss (IL) as shown in Figure 9. Quadrature level and nonlinearity can also be evaluated with open-loop measurements.

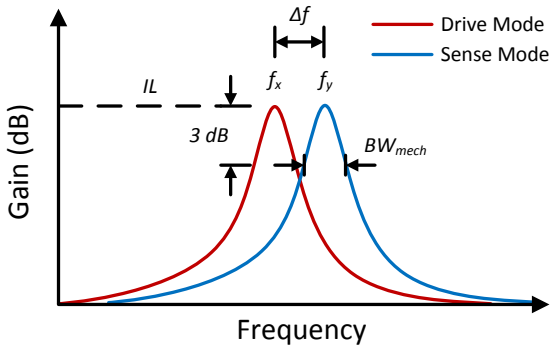


Figure 9 – Illustration of an open-loop measurement showing insertion loss, 3 dB bandwidth, and mode split.

The IL is the measurement of power loss from the input to the output, and it is observed as the dB level of the resonant peak in open-loop characterization. Through open-loop measurements, evidence of proper device transduction, mode-matching, quadrature compensation, and other gyro characteristics can be seen to provide a means for manual

characterization. Measuring the phase transition at the resonant mode is also useful for finding the desired lock-in phase to successfully track frequency changes in closed-loop operation as demonstrated by Figure 10.

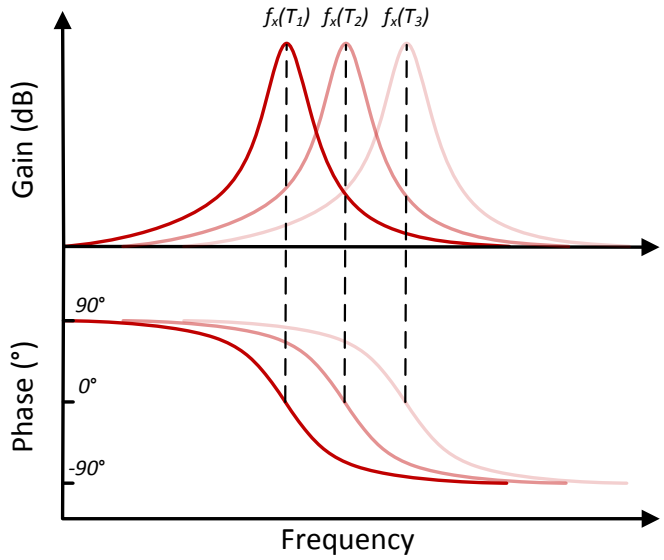


Figure 10 – Illustration of the phase-frequency gyro relationship. It is demonstrated that when locked in at the phase of the resonant peak, tracking phase changes allows for the tracking of frequency as is drifts with temperature.

For enhanced troubleshooting capabilities in the field, it is beneficial to use an all-digital architecture that is compatible with both open-loop and closed-loop, and an FPGA-based implementation provides a means for such systems.

2.3 Closed-Loop Gyroscope Operation

Closed-loop operation enables rate readout. In many traditional analog implementations of closed-loop gyroscope implementations, a self-sustained drive loop architecture by scaling the output signal using an automatic gain controller (AGC) and phase shifter to modify the output signal. To satisfy the Barkhausen criterion for sustained oscillation [33], which requires the gain and phase of the feedback signal to be 1 V/V and 360°, respectively. The AGC uses a peak detector, proportional-integral (PI) controller,

and variable gain amplifier (VGA) to scale the velocity output for mode actuation. To extract the rate output, the signal is then demodulated with analog mixers by using a combination of phase shifters or a phase-locked loop (PLL) circuit to provide the in-phase and out-of-phase demodulation signals. Using a digital platform, a self-sustained drive loop is achieved by monitoring the signal phase, and since the inflection point of the phase response maintains aligned with the resonant frequency as the frequency drifts, actuation signal frequency can be adjusted accordingly, and details of the digital architecture implementation are given in Chapter 4.

2.4 Compensation Methods

In many advanced gyro systems, it is desirable to match the gyroscopic frequency of each mode and to compensate for mode misalignment. It has been shown in equation 1.10 that applying a polarization voltage to a resonating body results in an amplitude-modulated force (F_{Ti}) that alters the effective frequency of a resonant mode. By applying a DC tuning voltage (V_{Ti}) to an electrode aligned with the antinode of a gyroscopic mode, the voltage difference enables the manual adjustment of individual modes to achieve mode-matched condition as shown in the equations below:

$$F_{Ti} = \frac{1}{2} \cdot \frac{\varepsilon_0 A_{el}}{(x - g_0)^2} \cdot (V_P - V_{Ti})^2 \approx \frac{C_{0i}(V_P - V_{Ti})^2}{{g_0}^2} x \tag{2.3}$$

$$\begin{aligned} \ddot{x} + \frac{\omega_x}{Q_x}\dot{x} + \left({\omega_x}^2 - \frac{1}{m} \cdot \frac{C_0(V_P - V_{Tx})^2}{{g_0}^2}\right) x &= \frac{1}{m} \cdot \frac{C_0 V_P}{g_0} \cdot v_0 \cos(\omega t) \\ \ddot{y} + \frac{\omega_y}{Q_y}\dot{y} + \left({\omega_y}^2 - \frac{1}{m} \cdot \frac{C_0\left(V_P - V_{Ty}\right)^2}{{g_0}^2}\right) y &= 2\lambda \Omega_z \dot{x} \end{aligned} \tag{2.4}$$

In a similar way that the electrostatic spring-softening effect adjusts the effective resonant frequency of the gyro modes, it can also null the mode misalignment terms (ω_{xy})

to reduce the quadrature coupling signal. By applying voltages to a set of electrodes placed between the antinodes of the gyroscopic modes (V_{Qi}), as shown in Figure 11, the stiffness coupling terms can be nulled, and the phase angle of modal coupling determines which set of electrodes to use for mode alignment [34]. The equation illustrating this function is also shown by equation 2.5.

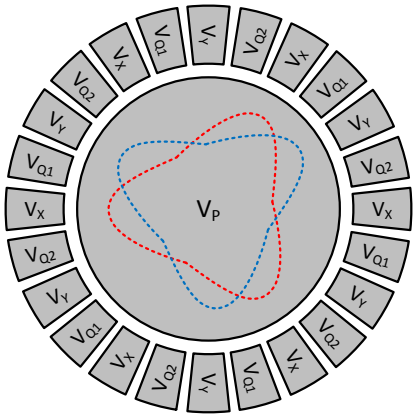


Figure 11 – Electrode configuration for a 24-electrode BAW gyroscope.

$$\ddot{x} + \frac{\omega_x}{Q_x}\dot{x} + \left({\omega_x}^2 - \frac{1}{m}\cdot\frac{C_0{V_P}^2}{{g_0}^2}\right)x + \frac{\omega_{xy}}{Q_{xy}}\dot{y} + \left({\omega_{xy}}^2 - \frac{1}{m}\cdot\frac{C_0\left(V_P - V_{Qi}\right)^2}{{g_{0xy}}^2}\right)y = \frac{F_x}{m}\cos(\omega t) - 2\lambda\Omega_z\dot{y}$$
$$\ddot{y} + \frac{\omega_y}{Q_y}\dot{y} + \left({\omega_y}^2 - \frac{1}{m}\cdot\frac{C_0{V_P}^2}{{g_0}^2}\right)y + \frac{\omega_{xy}}{Q_{xy}}\dot{x} + \left({\omega_{xy}}^2 - \frac{1}{m}\cdot\frac{C_0\left(V_P - V_{Qi}\right)^2}{{g_0}^2}\right)x = 2\lambda\Omega_z\dot{x} \quad (2.5)$$

To reduce the effects of mode split and mode misalignment temperature compensation is commonly implemented to vary the tuning and alignment voltages for bias and scale factor error reduction across temperature. Using a look-up table-based approach provides a means for compensation; however, it relies on factory calibration measurements that are prone to becoming inaccurate over time due to the aging of the device while also increasing the cost. The most favorable option would be to implement various layers of calibration to reduce the bias and scale factor errors over time and temperature.

CHAPTER 3: GYROSCOPE INTERFACING ARCHITECTURES

Various gyroscope interfacing architectures can be used depending on the desired features versus ease of implementation. The universal interfacing scheme for rate gyroscopes is the conventional gyro architecture that was demonstrated in the previous chapters. Various compensation methods for automatic mode-matching and quadrature compensation have been presented, but the complexity of control and lack of scale factor calibration limit the effectiveness of these methods as solutions for high-grade gyroscopes [35]-[37]. Mode reversal is also a method used to essentially characterize the ZRO by alternating the roles of the gyroscopic modes between drive and sense [38], [39]. While mode reversal can effectively cancel long-term bias drift, it requires a period of offline calibration which could potentially induce errors in the gyro output. Advanced packaging techniques have also been shown in which the gyro is mounted to a rotating stage to provide a self-contained means for calibration [40], but they are limited in their practicality due to their complexity.

Alternative interfacing methods have also been developed to provide in-run calibration for bias and scale factor, but while providing enhancements in long-term drift, they are limited in their abilities to provide a low-noise rate readout. One such method is that of a phase-modulated architecture, mentioned in [41] and [42], that provides a virtual rate to characterize scale factor with no physical rate being applied. This architecture is limited in that it cannot simultaneously provide both physical rate and virtual rate as it requires offline scale factor characterization, and it also does not provide a means for bias calibration. Frequency-modulated interfacing architectures have been presented in [43]-

[46] to provide a means for bias and scale factor calibration. Since the rate readout with this design methodology is ratiometric, it inherently shows low sensitivity to environmental conditions providing good performance for long-term drift for bias and scale factor; however, in these cases, the resolution is increased limiting the practicality of such architectures.

While various alternative architectures address long-term drift in bias and scale factor, they are limited in their ability to measure low angular rate. Using the dual-mode architecture, in-run bias cancellation, automatic mode-matching, and scale factor calibration is made possible while showing promising potential for low-noise operation. The details of the single-mode and dual-mode schemes are discussed in this chapter.

3.1 Conventional Gyroscope Architecture

The conventional (single-mode) gyro scheme is the typical method for interfacing rate gyroscopes [47]. While some methods for in-run compensation have been shown to reduce quadrature error and maintain mode-matched condition, using conventional gyro operation limits the user's ability to provide extensive in-run closed-loop calibration. One advantage of conventional operation is that it can be used for virtually any Coriolis vibratory gyroscope where other gyroscope architectures may prefer a specific device design, and a basic conceptual diagram is shown in Figure 12.

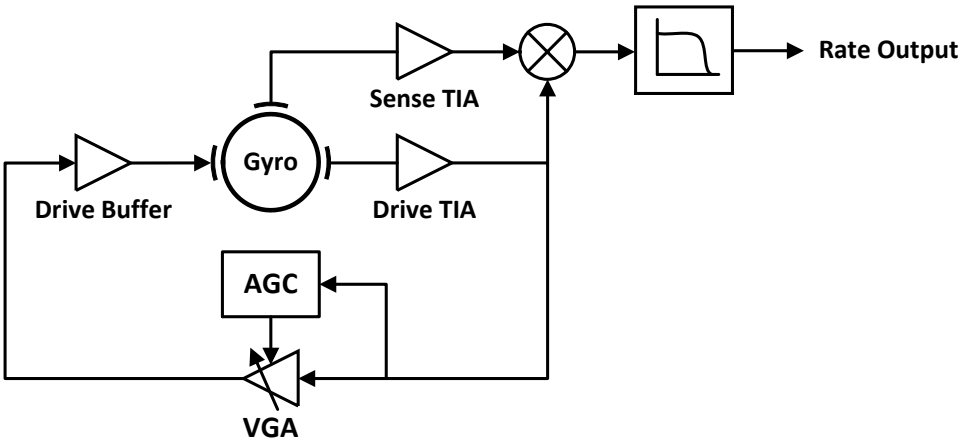


Figure 12 – Basic diagram of the conventional (single-mode) interfacing architecture.

3.1.1 Drive Loop Implementation

The drive mode of a conventional gyro architecture is actuated into oscillation with a sinusoidal signal at the resonant frequency of the drive mode. Sustained drive oscillation can be achieved by either implementing an analog or digital drive loop. The analog drive loop requires use of an AGC and VGA to rescale the gyro output signals as mentioned in Chapter 2, but by using a digital implementation, the signal can be generated independently with high-resolution frequency adjustability. In a mode-matched, mode-aligned gyro, the phase response of the voltage input to current output transfer function transitions from +90° to -90°, ideally, with the 0° point at the gyro resonant frequency, but in practical cases, additional phase delay will be seen due to the analog front-end and parasitic capacitances. To maintain oscillation at the resonant frequency, the phase at the resonant peak must be characterized to be used as the setpoint for the closed-loop drive scheme. The pick-off TIAs of the drive signal give a transfer function of R_F, and by reading out differential gyro signal outputs, it is doubled to $2 \cdot R_F$. The total transfer function between the voltage output ($V_{d,out}$) and voltage input ($V_{d,in}$) of the drive mode can be described by combining equation 1.5, 1.10, and 1.13 to yield:

$$\frac{V_{d,out}}{V_{d,in}} = \frac{F_x(j\omega_x)}{V_{d,in}(j\omega_x)} \cdot \frac{X(j\omega_x)}{F_x(j\omega_x)} \cdot \frac{I(j\omega_x)}{X(j\omega_x)} \cdot \frac{V_{d,out}}{I(j\omega_x)}$$
$$\frac{V_{d,out}}{V_{d,in}} = (\eta) \cdot \left(-j\frac{Q_x}{m{\omega_x}^2}\right) \cdot (j\omega_x\eta) \cdot (2R_F) = \frac{2Q_x\eta^2 R_F}{m\omega_x} \tag{3.1}$$

3.1.2 Sense Channel Demodulation

The rate signal is picked off as an amplitude-modulated waveform at the gyro's resonant frequency with the signal amplitude proportional to rate. By combining the concept of equation 3.1 with the Coriolis-induced mode coupling shown in 1.5, the rate-induced amplitude of the sense signal is described below:

$$\frac{V_{s,out}}{V_{d,in}} = \frac{F_x(j\omega_x)}{V_{d,in}(j\omega_x)} \cdot \frac{X(j\omega_x)}{F_x(j\omega_x)} \cdot \frac{Y(j\omega_x)}{X(j\omega_x)} \cdot \frac{I(j\omega_x)}{Y(j\omega_x)} \cdot \frac{V_{s,out}}{I(j\omega_x)}$$
$$\frac{V_{s,out}}{V_{d,in}} = (\eta) \cdot \left(-j\frac{Q_x}{m{\omega_x}^2}\right) \cdot \left(\frac{2\lambda\Omega_z Q_y}{\omega_x}\right) \cdot (j\omega_x\eta) \cdot (2R_F) = \frac{4\lambda Q_x Q_y \eta^2 R_F}{m{\omega_x}^2}\Omega_z \tag{3.2}$$

The signal is then demodulated using a reference waveform with amplitude A at the same frequency to provide a low-pass filtered DC output (V_Ω) proportional to rate:

$$\begin{aligned} V_\Omega &= LPF\{A\cos(\omega_x t) \times |V_{s,out}|\cos(\omega_x t)\} \\ &= LPF\left\{\frac{4\lambda Q_x Q_y \eta^2 R_F |V_{d,in}|}{m{\omega_x}^2}\Omega_z \cdot \left[\frac{A}{2} + \frac{A}{2}\cos(2\omega_x t)\right]\right\} \\ &= \frac{2A\lambda Q_x Q_y \eta^2 R_F |V_{d,in}|}{m{\omega_x}^2}\Omega_z \end{aligned} \tag{3.3}$$

Using look-up table (LUTs), drift in mechanical characteristics such as frequency, quality factor, frequency split, and stiffness coupling can be temperature compensated with factory calibration measures.

3.2 Dual-Mode Gyroscope Architecture

With the dual-mode architecture, calibration layers can be implemented to provide in-run scale factor calibration and automatic mode-matching, and inherent bias cancellation is also made possible [48], [49]. Through applying actuation forces to both gyroscopic modes, the presence of residual stiffness coupling and damping coupling is canceled in the output based on the assumption of an axisymmetric structure. The cancellation of the bias-contributing terms is accomplished by locking into the phase at the peak of the summation output and detecting rate through the difference output as shown in Figure 13. The most basic system of equations that assumes mode-matched condition, equal quality factor, and no stiffness or damping coupling as shown below:

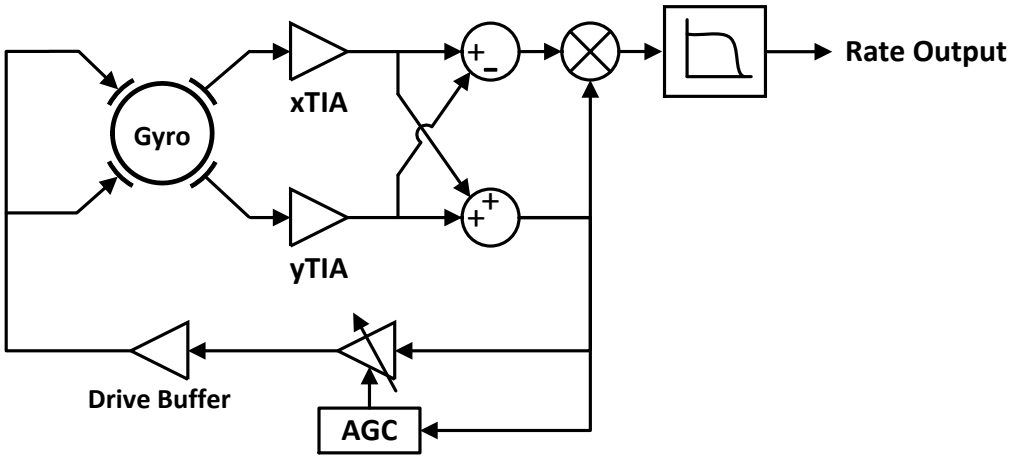


Figure 13 – Basic diagram of the dual-mode interfacing architecture.

$$\begin{bmatrix} j\frac{{\omega_0}^2}{Q} & j\omega 2\lambda\Omega_z \\ -j\omega 2\lambda\Omega_z & j\frac{{\omega_0}^2}{Q} \end{bmatrix} \cdot \begin{bmatrix} X \\ \\ Y \end{bmatrix} = \begin{bmatrix} \frac{F_0}{m} \\ \\ \frac{F_0}{m} \end{bmatrix} \tag{3.4}$$

This equation can then be solved and processed to give the summation and difference outputs of *x* and *y* displacement:

$$X_{SUM} = X + Y = \frac{-j\frac{2\omega_0}{Q}}{\left(\frac{\omega_0}{Q}\right)^2 + (2\lambda\Omega_z)^2} \cdot \frac{F_0}{m\omega_0}$$
$$X_{DIFF} = X - Y = \frac{-j4\lambda\Omega_z}{\left(\frac{\omega_0}{Q}\right)^2 + (2\lambda\Omega_z)^2} \cdot \frac{F_0}{m\omega_0} \quad (3.6)$$

3.2.1 Inherent Bias Cancellation

In this architecture, forces are applied to each mode to be added and subtracted for closed-loop operation with enhanced rate readout. When considering the non-ideal gyro model, the equation for can be represented as:

$$\begin{bmatrix} {\omega_x}^2 - \omega^2 + j\omega\frac{\omega_x}{Q_x} & {\omega_{xy}}^2 + j\omega\left(\frac{\omega_{xy}}{Q_{xy}} + 2\lambda\Omega_z\right) \\ {\omega_{xy}}^2 + j\omega\left(\frac{\omega_{xy}}{Q_{xy}} - 2\lambda\Omega_z\right) & {\omega_y}^2 - \omega^2 + j\omega\frac{\omega_y}{Q_y} \end{bmatrix} \cdot \begin{bmatrix} X \\ Y \end{bmatrix} = \begin{bmatrix} \frac{F_x}{m} \\ \frac{F_y}{m} \end{bmatrix} \quad (3.4)$$

To demonstrate the inherent bias cancellation of the dual-mode architecture, we assume that in equation 3.4, $\omega_0=\omega_x=\omega_y$, and we solve to yield the following relationships for mode displacement:

$$X = \frac{-jQ_xF_x + \left[\frac{{\omega_{xy}}^2}{\omega_0} + j\left(\frac{\omega_{xy}}{Q_{xy}} + 2\lambda\Omega_z\right)\right]\frac{Q_xQ_y}{\omega_0}F_y}{1 + \frac{Q_xQ_y}{{\omega_0}^2}\left[\left(\frac{{\omega_{xy}}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2\right]}$$
$$Y = \frac{\left[\frac{{\omega_{xy}}^2}{\omega_0} + j\left(\frac{\omega_{xy}}{Q_{xy}} - 2\lambda\Omega_z\right)\right]\frac{Q_xQ_y}{\omega_0}F_x - jQ_yF_y}{1 + \frac{Q_xQ_y}{{\omega_0}^2}\left[\left(\frac{{\omega_{xy}}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2\right]} \quad (3.5)$$

Since the bias contributing terms, ω_{xy} and Q_{xy}, are common mode and the rate terms are differential, by taking the sum and difference, enhanced drive and rate outputs are made available. To demonstrate bias cancellation, equal force ($F_x=F_y=F_0$) and quality factor ($Q_x=Q_y=Q$) is assumed. The summation output provides a means for closed-loop operation since it eliminates the rate terms in the numerator to provide a rate-independent phase output, and the difference output provides an enhanced rate output that rejects bias terms:

$$X_{SUM} = X + Y = \frac{-j\frac{2\omega_0}{Q} - 2\left(\frac{{\omega_{xy}}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)}{\left(\frac{\omega_0}{Q}\right)^2 + \left(\frac{{\omega_{xy}}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2} \cdot \frac{F_0}{m\omega_0}$$
$$X_{DIFF} = X - Y = \frac{-j4\lambda\Omega_z}{\left(\frac{\omega_0}{Q}\right)^2 + \left(\frac{{\omega_{xy}}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2} \cdot \frac{F_0}{m\omega_0} \quad (3.6)$$

In practical cases, quality factor equality may not be assumed; therefore, to compensate for Q-mismatch, the actuation forces are adjusted to satisfy the condition: $Q_xF_x=Q_yF_y$.

3.2.2 Automatic Mode-Matching

To provide closed-loop automatic mode-matching functionality, the demodulated I and Q channels provide rate and mode split information, respectively. The modes can be matched by adjusting the tuning voltage to null the mode-split indicator channel. Mode split ($\Delta\omega=\omega_y-\omega_x$) is modeled in the gyro equations, and it can be assumed that $\Delta\omega<<\omega_0$, $\omega_0=(\omega_x+\omega_y)/2$, $F_x=F_y=F_0$, and $Q_x=Q_y=Q$ are valid for simplification. Based on this assumption, equation 3.4 can be solved to provide summation and difference outputs that account for mode split:

$$X_{SUM} = X + Y = \frac{-j\frac{2\omega_0}{Q} - 2\left(\frac{\omega_{xy}{}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)}{\Delta\omega^2 + \left(\frac{\omega_0}{Q}\right)^2 + \left(\frac{\omega_{xy}{}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2} \cdot \frac{F_0}{m\omega_0}$$

$$X_{DIFF} = X - Y = \frac{-2\Delta\omega + j4\lambda\Omega_z}{\Delta\omega^2 + \left(\frac{\omega_0}{Q}\right)^2 + \left(\frac{\omega_{xy}{}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + (2\lambda\Omega_z)^2} \cdot \frac{F_0}{m\omega_0} \tag{3.7}$$

Since the mode-split indicator and rate output are 90° out of phase, they are easily separated through I/Q demodulation; therefore, the mode-split indicator can be reduced to zero by controlling the tuning voltage as shown in Figure 14.

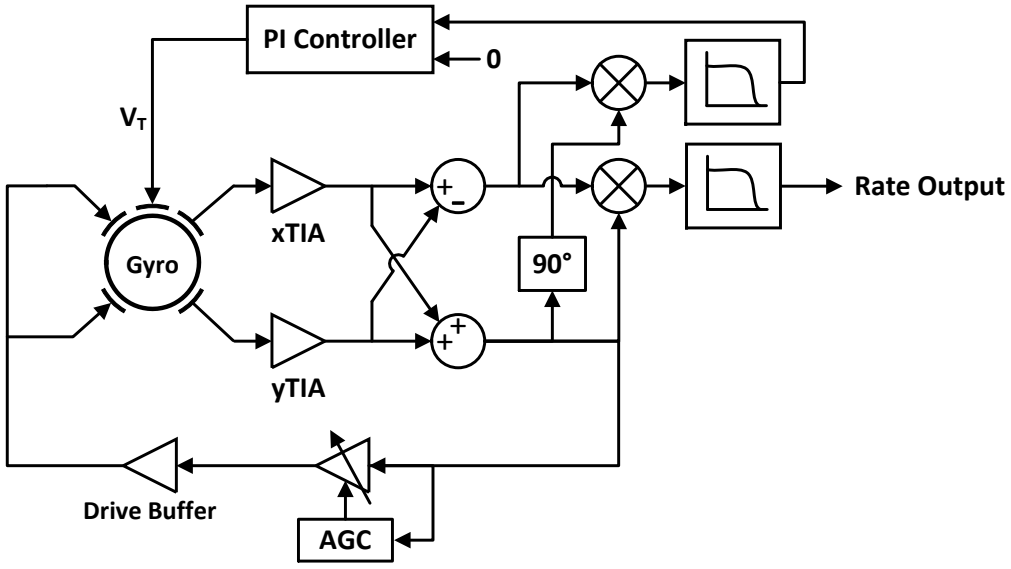


Figure 14 – Automatic mode-matching diagram showing the active tuning to keep the mode-split indicator output at zero.

3.2.3 Scale Factor Calibration

By applying a virtual calibration stimulus, the raw rate output value can be continually rescaled to keep the scale factor stable across time and temperature. Virtual rate is applied through a user-defined calibration signal (V_{CAL}) that scales the amplitude of

the mode velocity outputs from the TIAs. This signal is added to the actuation voltage to provide a net actuation force to each gyroscopic mode as shown in equation 3.8 and Figure 15.

$$F_x(t) = \eta[v_0 \cos(\omega_0 t) - \eta R_F V_{CAL} \dot{y}] = F_0(t) - \eta^2 R_F V_{CAL} \dot{y}$$
$$F_y(t) = \eta[v_0 \cos(\omega_0 t) + \eta R_F V_{CAL} \dot{x}] = F_0(t) + \eta^2 R_F V_{CAL} \dot{x} \quad (3.8)$$

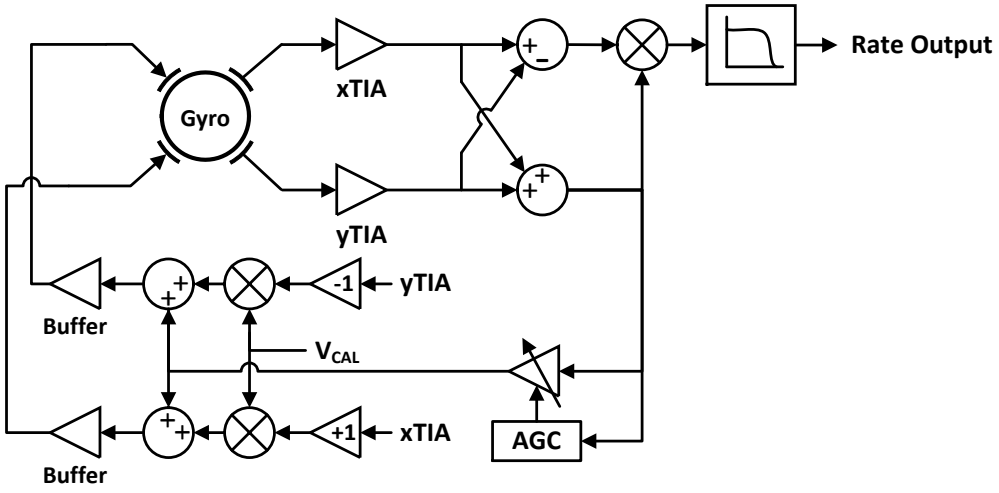


Figure 15 – Scale factor calibration diagram showing the combination of the velocity feedback from the TIAs and a calibration stimulus being applied to the input channel of the gyro.

Due to the superposition property of virtual rate and physical rate, the virtual rate appears in the output similarly to physical rate, and the scale factor of virtual rate changes with a common trend to that of physical rate. By substituting the actuation forces of equation 3.8 into the dual-mode gyro model and assuming equal quality factor and mode-matched condition, the summation and difference of displacements terms can be shown as:

$$X_{SUM} = X + Y = \frac{-j\frac{2\omega_0}{Q} - 2\left(\frac{\omega_{xy}{}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)}{\left(\frac{\omega_0}{Q}\right)^2 + \left(\frac{\omega_{xy}{}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + \left(2\lambda\Omega_z + \frac{\eta^2 R_F V_{CAL}}{m}\right)^2} \cdot \frac{F_0}{m\omega_0}$$

$$X_{DIFF} = X - Y = \frac{-j2 \cdot \left(2\lambda\Omega_z + \frac{\eta^2 R_F V_{CAL}}{m}\right)}{\left(\frac{\omega_0}{Q}\right)^2 + \left(\frac{\omega_{xy}{}^2}{\omega_0} + j\frac{\omega_{xy}}{Q_{xy}}\right)^2 + \left(2\lambda\Omega_z + \frac{\eta^2 R_F V_{CAL}}{m}\right)^2} \cdot \frac{F_0}{m\omega_0} \quad (3.9)$$

This calibration scheme provides a valuable means for the reduced dependence on factory calibration steps. Rather than requiring extensive characterization of voltage as it translates to angular rate, only a baseline measurement is needed, and the known virtual stimulus can track changes in the scale factor definition as shown in the relationship below:

$$SF_{calibrated,x} = SF_{virtual,0} \cdot \frac{SF_{physical,0}}{SF_{virtual,x}} \quad (3.10)$$

$SF_{virtual,0}$ and $SF_{physical,0}$ are the baseline measurements, and the change seen in the virtual stimulus ($SF_{virtual,x}$) allows for calibration in the physical rate readout. This thesis primarily focuses on the dual-mode architecture and its implementation on a digital platform.

CHAPTER 4: DIGITAL ARCHITECTURE IMPLEMENTATION

The conventional and dual-mode interfacing architectures were implemented on a digital platform to provide a means for side-by-side comparison in system performance. The digital architecture was implemented on a FlexRIO system built by National Instruments (NI) that integrates both a field-programmable gate array (FPGA) and a real-time (RT) controller, and the system components are shown in Figure 16. To mitigate the need for drift-inducing analog electronics, such as mixers and phase shifters, analog signals are converted to the digital domain with an NI adapter module. In the digital domain, processing of these signals can be more extensive without increasing the number of components that are prone to drift, and it allows for a more user-friendly interface.

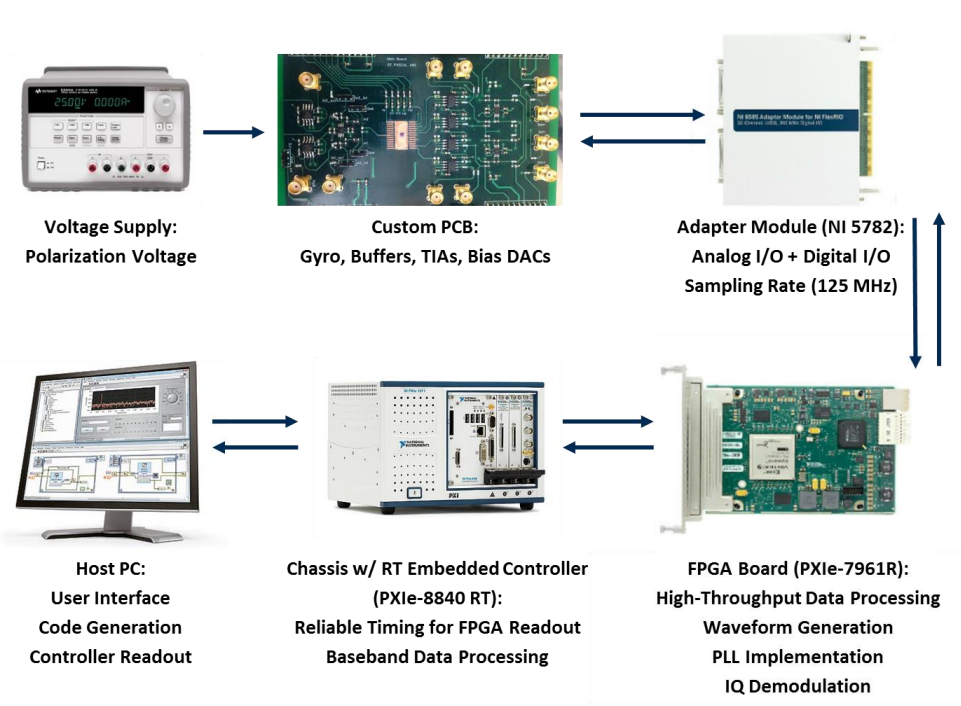


Figure 16 – Equipment used for implementation of the digital architecture.

A module containing an FPGA of the Virtex-5 family was used with a data conversion adapter module to provide a platform for high-speed digital processes for data acquisition, signal conditioning, and signal generation. The digital data is streamed from the FPGA to a dual-core RT controller using the high-bandwidth PXI express (PXIe) platform of the chassis. The chassis, that houses the system components, allows for a bandwidth of ~1 GB/s and defines the streaming capacity from FPGA to RT controller. The RT controller provides a means for processes requiring relatively low data rates such as data collection, mathematical calculations, data analysis, and user adjustments. The diagram of digital architecture is shown in Figure 17, and further details of the digital architecture are given in this chapter.

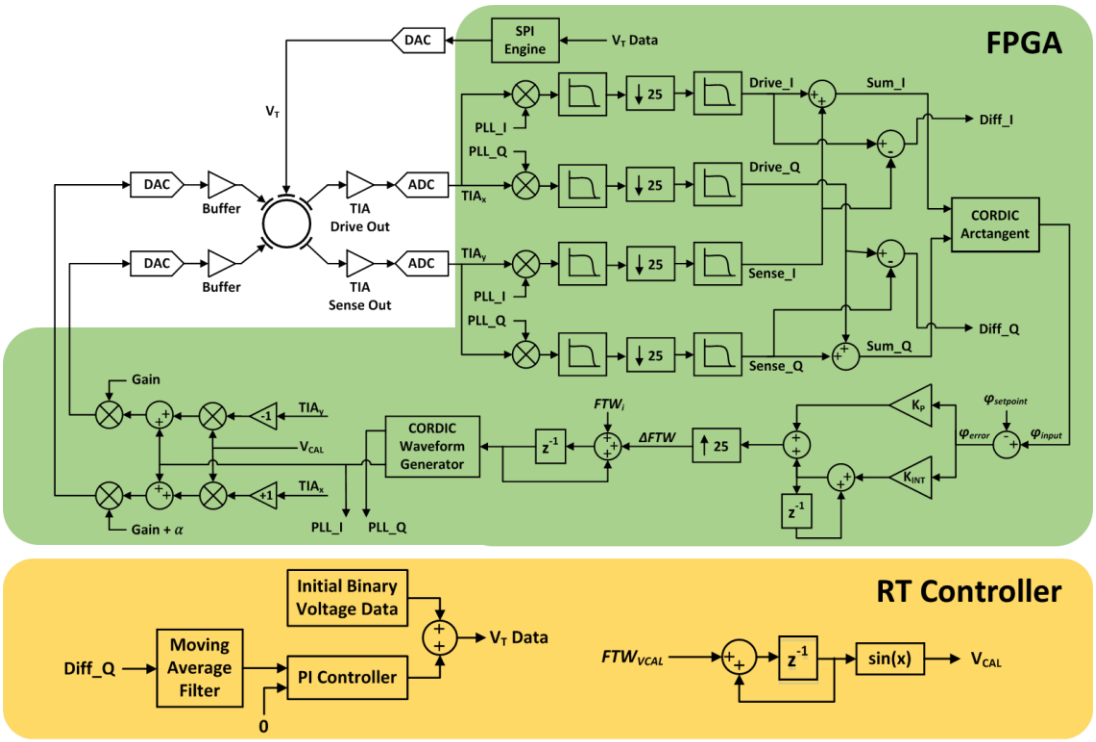


Figure 17 – Diagram showing the implementation of the digital architecture on the FPGA and real-time controller platform

4.1 FPGA Design and Considerations

LabVIEW FPGA provides a graphical means for FPGA programmability. The high-throughput FPGA functions are developed in block diagram form where the data rate is defined by the timing structures. The block diagram codes are converted to VHDL and compiled to produce the bitfile that is used for digital circuit integration on the FPGA. To ensure all functions within the loop are executed at every clock cycle, a single-cycle timed loop (SCTL) can be used, and for the timing to be determined by the logic, a while loop can be used. The SCTL is used for functions that handle time-sensitive data which makes it suitable for high-frequency data conversions and signal processing, and using an FPGA enables parallel processing for various operations within the architecture [50], [51].

4.1.1 FPGA Resources

The FPGA used in this system is the Virtex-5 SX50T with 8,160 FPGA slices, 288 DSP slices, and 4,752 kb of block RAM. The most basic building blocks for FPGA designs are the FPGA slices, containing LUTs and registers, to provide combinatorial and synchronous logic functionality. For many high-speed data processes, these FPGA slices may not provide suitable data rates, and for faster performance, DSP slices can be used. With dedicated multipliers and adders, DSP slices have proven to be useful for the implementation of filters and other signal processes to provide the desired speed while also reducing the consumption of other resources. For proper usage of resources, the handling of data through the signal chain must also be considered. At various points throughout the signal chain, values must be rounded to prevent excessive resource consumption without excessively increasing quantization error. While simple data truncation requires no

additional logic for implementation, it can induce offset in the rounded data, and in cases where sensitive signal are being handled, round half-even is used. When using round half-even, the initial value is rounded to the nearest even number to reduce offset in the resulting values when compared to other rounding methods. Another common practice when implementing designs with FPGAs is the use of a fixed-point numbers in lieu of floating-point. Using fixed-point values allows for integer data to be presented as decimals to allow for easier implementation of mathematical functions. Fixed-point format has a user-defined fractional word length and integer word length, in contrast to floating-point. For floating point the total word length is defined, but the decimal location changes depending on the numerical value. By simulating a design with a floating-point number format, the designer can gain a sense of the required fixed-point settings and rounding requirements for a high-performance hardware implementation with minimal resource consumption.

4.1.2 Timing Considerations

FPGAs allow for high-speed, high-throughput data processes, and the clocks available for the system detailed in this thesis are 250 MHz, 200 MHz, and 40 MHz. Additional clocks can be derived using the digital clock managers (DCMs) that are included in the hardware of the FPGA. To pass the timing requirements of any given design, logic and routing delays between registers must be within the period of the clock cycle. Two key techniques frequently used to alleviate timing demands are the implementation of high-throughput DSP blocks and the use of pipelining stages. High-throughput implementations of mathematical operations help reduce logic delay, and by pipelining the designs, the operations executed per clock cycle can be customized. This is done by placing registers between combinatorial logic blocks to build a sequential process.

While pipelining increases latency and resource consumption, it is, in many cases, necessary for high-speed logic implementation.

4.2 Data Conversion

To interface MEMS gyroscopes with a digital architecture, data converters are used to generate analog actuation signals and to convert the gyro output signals to the digital domain. In subsection 2.1.2, it was shown that for low-noise data conversion, converters must have high bit resolutions and high sampling rates. The adapter module from National Instruments (NI 5782) uses an on-board clock distribution chip from Analog Devices (AD9512) to provide low-jitter clocking for the data converters. The ADCs and DACs were also implemented on the NI 5782, and the data converter specifications are reported in the following subsections.

4.2.1 Digital-to-Analog Conversion

Sinusoidal signals are converted to the analog domain for the scalable actuation of the gyroscopic modes. The part used in this system is the DAC5682Z, a 16-bit dual-DAC available from Texas Instruments. Due to the relatively high frequency modes of the BAW gyroscope (~2.6 MHz), a high OSR is needed to keep the quantization noise low, and the sampling rate is 125 MHz for an OSR of ~24. A current-steering DAC must be used to achieve these high data rates, but it is limited in linearity and resolution compared to many low-frequency precision DACs. It will be shown in Chapter 5 that the DACs heavily influence the noise performance of the gyroscope.

4.2.2 Analog-to-Digital Conversion

The gyro output signals are converted to the digital domain through implementation of ADCs with a common sampling rate to that of the DACs. The dual-channel ADC used is the ADS62P49, a 14-bit data converter available from Texas Instruments. The ADC used in this design is a pipelined ADC to provide a fast sampling rate for a high OSR. Similarly to the current-steering DACs, pipelined ADCs do not provide superior linearity or resolution. To overcome the limitations, any harmonics generated due to nonlinearity can be filtered in the signal chain, and the increased OSR helps to overcome the resolution limitations.

4.3 Gyroscope Signal Chain

In the signal chain, a sinusoidal waveform is generated and scaled before being converted to the analog domain to enable gyroscope actuation. The gyroscope output signals are then converted to the digital domain where they are processed to extract amplitude and phase information for rate readout and closed-loop operation. This section addresses the DSP measures that were taken in the design of the signal chain to ensure that they not only exhibit low drift but also do not excessively consume FPGA resources.

4.3.1 Waveform Synthesis

The sine and cosine waveforms are generated to output the gyroscope actuation signal through the DACs and to demodulate the pick-off signals from the ADCs. Waveform synthesis, often referred to as direct digital synthesis (DDS), is achieved through use of a coordinate rotation digital computer (CORDIC). The CORDIC algorithm is an iterative solver for trigonometric functions that provide improved frequency selectivity than an LUT-based waveform generator. Signals can only be defined with a finite number of values

saved in FPGA memory using an LUT-based waveform generator. With a CORDIC-based approach, only a small number of LUTs is required to provide initial values for iterative calculations to provide a significantly improved frequency resolution.

Both forms of waveform synthesis require a sawtooth phase input from a phase accumulator, and in both cases this phase accumulator uses an adder and a flip-flop to increment the phase input value at the rising edge of the clock. The phase input of a LUT-based form of DDS is simply a bit-by-bit accumulation of values to provide the memory address for the predetermined waveform data. The CORDIC-based DDS method uses an integer with a given word length as the phase input to determine frequency based on the value added to the input at each clock cycle, known as the frequency tuning word (*FTW*). In this case, the sinusoidal frequency (f_{sig}) is defined by the clock frequency (f_{clk}), input word length (*M*), and *FTW* as shown in the following relationship:

$$f_{sig} = \frac{f_{clk}}{2^M} \cdot FTW \tag{4.1}$$

Using this approach allows for superior frequency resolution to accurately follow the gyroscope's resonant frequency across temperature, and using this method results in precise sinusoidal waveforms that are able to be adjusted without signal discontinuities and without sacrificing excessive FPGA resources.

4.3.2 Digital Signal Demodulation and Filtering

Digital signal demodulation makes use of zero-drift digital multipliers to overcome the limitations of its analog mixer counterparts. In the case of this architecture, I/Q

demodulation is used to extract in-phase and quadrature-phase components of the gyro signals. Since these signals are downconverted to baseband, they must be filtered to attenuate the residual high-frequency signal component from demodulation and to prevent noise folding when downsampled.

Downsampling, also decimation, is necessary to reduce the sampling rate of the downconverted data, and to prevent noise folding at each stage of downsampling, the Nyquist criteria must be satisfied [52]. The Nyquist criteria states that the sampling frequency must be greater than or equal to twice that of the signal frequency, and the same principle is applied to reject noise folding as demonstrated in Figure 18. Before a sequence of digital data is downsampled, the filter should be designed to have a stopband frequency of half the new sampling frequency after decimation.

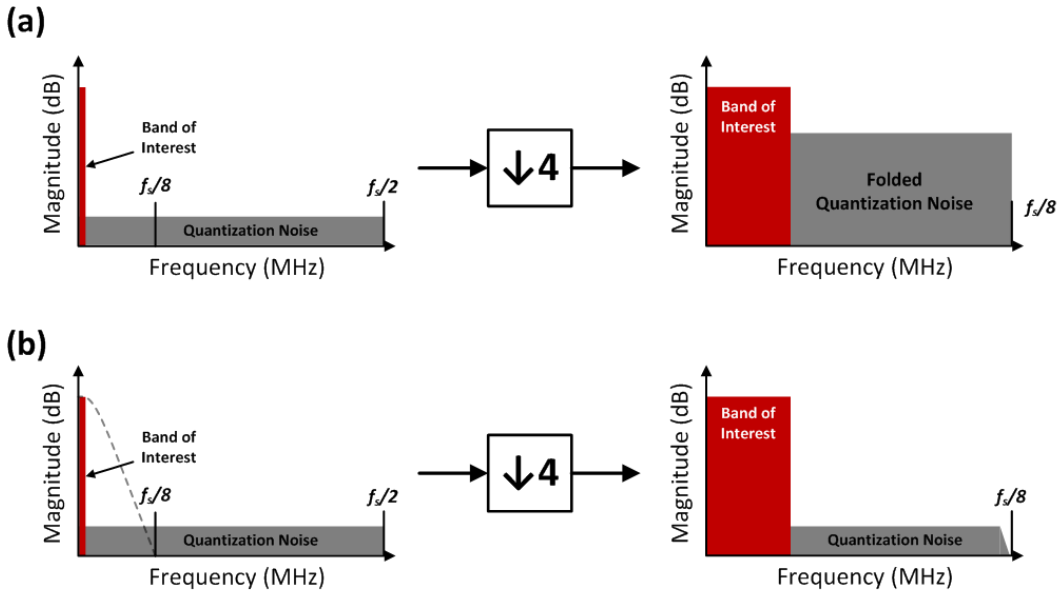


Figure 18 – Noise folding example with downsampling ratio of 4. (a) Case with no anti-aliasing filter; (b) Case with an anti-aliasing filter.

In this design, data converters operate at a high sampling rate of 125 MHz to prevent any quantization noise limitations. Operating at this data rate requires careful filter design to satisfy the demanding transfer function specifications without occupying excessive FPGA resources. The ideal filter solution would be that of a finite impulse response (FIR) filter. Since there are no recursive filter sections, FIR filters can easily operate at high data rates with less data truncation. The primary drawback of FIR filters is that they require an excessive amount of FPGA resources without providing a sufficient level of attenuation between the passband and stopband, as shown in Figure 19. In the design presented in this thesis, infinite impulse response (IIR) filters are used. With IIR filters, the anti-aliasing filters of each signal path can be implemented to reject noise folding without consuming excessive FPGA resources [53].

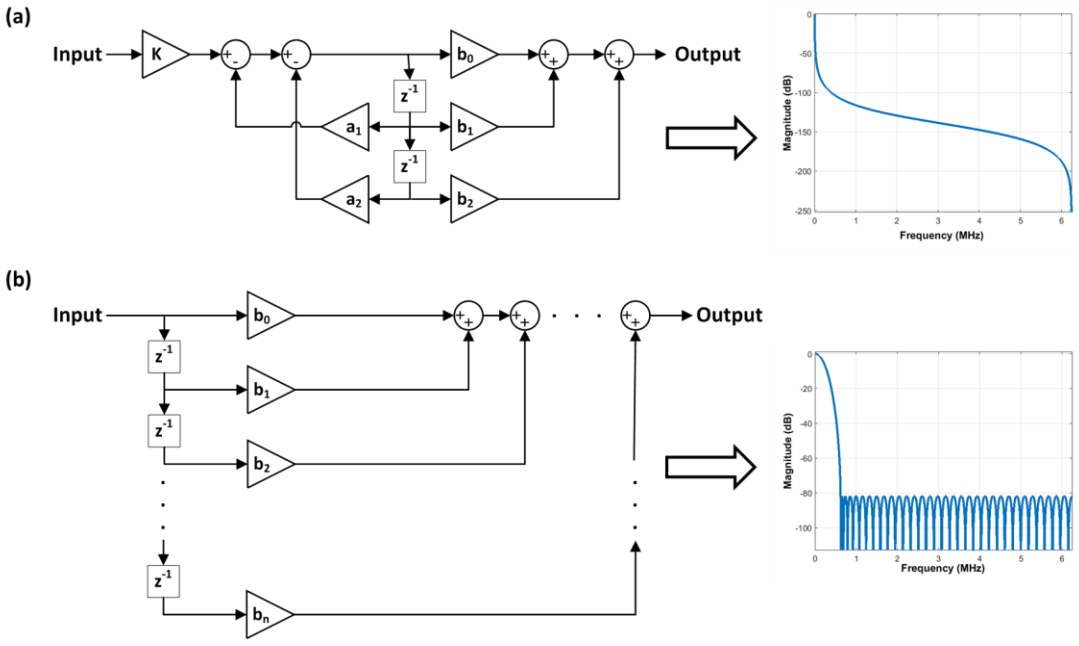


Figure 19 – (a) IIR Butterworth filter with the frequency response; (b) FIR equiripple single-rate filter with the frequency response.

While IIR filters can successfully alleviate resource consumption concerns, the logic delays of FPGA blocks are not well-suited for conventional IIR implementations at high data rates. Since the recursive paths have an increased number of logic operations to be executed in one clock cycle, the logic and routing delays are increased to make typical IIR filters incompatible with high-speed clocking. Timing requirements can be satisfied by redesigning the filters to have pipelined recursive stages. While simply adding flip-flops in this path would change the characteristics of the transfer function, adding cancelling poles and zeros allows for a pipelined IIR filter implementation that does not negatively alter the behavior of the filter response [54]. In this case, a 2nd-order IIR filter is converted to a pipelined IIR filter with recalculated coefficients demonstrated by Figure 20 and equation 4.2.

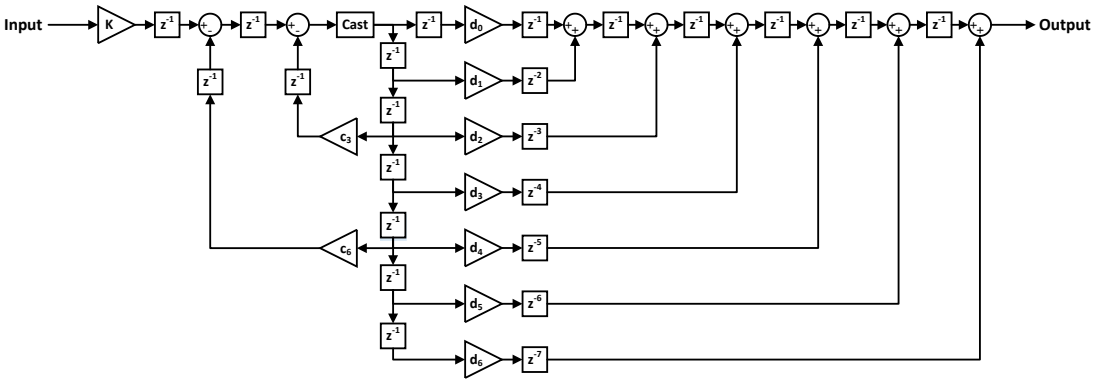


Figure 20 – Pipelined architecture for the high-throughput implementation of an IIR filter.

$$
\begin{aligned}
&H[z] = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2}}{1 + a_1 z^{-1} + a_2 z^{-2}} \\
&\longrightarrow H[z] = \frac{[1 - a_1 z^{-1} + ({a_1}^2 - a_2) z^{-2} - a_1 a_2 + {a_2}^2] \cdot [b_0 + b_1 z^{-1} + b_2 z^{-2}] \cdot z^{-9}}{1 - \left(3 a_1 a_2 - {a_1}^3\right) z^{-3} + {a_2}^3 z^{-6}} \\
&\longrightarrow H[z] = \frac{d_0 + d_1 z^{-1} + d_2 z^{-2} + d_3 z^{-3} + d_4 z^{-4} + d_5 z^{-5} + d_6 z^{-6}}{1 + c_3 z^{-3} + c_6 z^{-6}} \cdot z^{-9}
\end{aligned}
\tag{4.2}
$$

With the implementation of the improved filter, the data is decimated by a factor of 25, from 125 MHz to 5 MHz. At the decreased data rate, conventional IIR filters were able to be implemented without violating timing requirements, and at this point, the filtered data is transmitted to the RT controller for additional processing. The RT controller receives data at the rate of 10 kHz which translates to a decimation factor of 500 from the FPGA to the RT controller. At the controller level, one more stage of filtering and downsampling is implemented, and the final output operates at a 2 kHz data rate with a filter that defines the measurement bandwidth. The filter stages of the signal chain are illustrated by Figure 21.

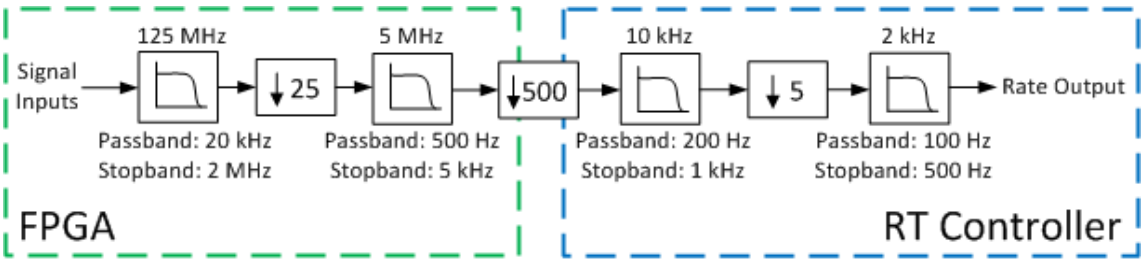


Figure 21 – Chain of anti-aliasing filters from signal demodulation to the rate output for a total down-sampling ratio of 62,500. Filter specifications and sampling rates are shown.

4.4 PLL-Based Drive Loop Architecture

PLLs are used to generate signals that are based on reference input signal, which makes them perfect for applications requiring stable sine and cosine signals for I/Q demodulation [55], [56]. They can be implemented in both the digital and analog domains, and the basic building blocks of a PLL are the phase detector, loop filter, and oscillator as shown in Figure 22.

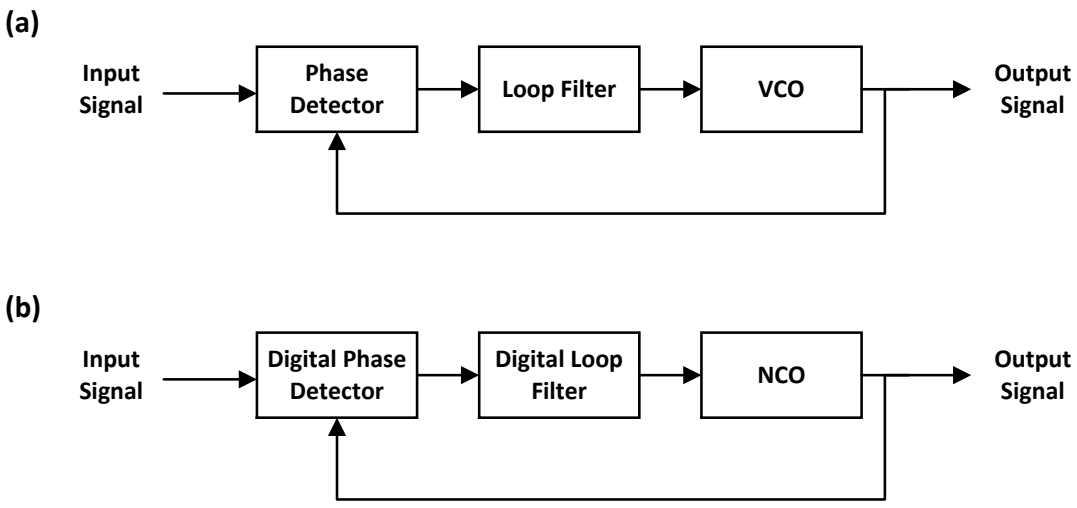


Figure 22 – (a) The basic block diagram for an analog PLL. (b) The basic block diagram for the all-digital PLL counterpart.

The phase detector compares the PLL output signal to the input signal, and the error between the signal phases is sent to the loop filter. A proportional-integral (PI) filter is typically used as the loop filter. This type of loop filter provides a dynamic output based on the difference between the phase error and phase setpoint to control the frequency of the oscillator that generates the resulting output signal.

4.4.1 Phase Detector

The phase detector in this implementation calculates the arctangent of the filtered I/Q signals from the drive or sum signal path to measure the phase at the gyroscope resonant frequency via open-loop analysis. Once the phase setpoint at the gyro peak is known, a CORDIC arctangent algorithm, implemented on the FPGA, is used to continually monitor the phase output of the gyroscope, and the series of equations that show the phase difference between the input and output signals of the gyro are shown below:

$$
\begin{aligned}
&A\sin(\omega t+\varphi) \xrightarrow{demod} \begin{cases} I_{channel}\colon A\sin(\omega t+\varphi)\times\sin(\omega t) \\ Q_{channel}\colon A\sin(\omega t+\varphi)\times\cos(\omega t) \end{cases} \\
&= \begin{cases} I_{channel}\colon \frac{A}{2}[\cos(\varphi)-\cos(2\omega t)] \\ Q_{channel}\colon \frac{A}{2}[\sin(\varphi)+\cos(2\omega t)] \end{cases} \xrightarrow{LPF} \begin{cases} I_{channel}\colon \frac{A}{2}\cos(\varphi) \\ Q_{channel}\colon \frac{A}{2}\sin(\varphi) \end{cases} \\
&\varphi = \tan^{-1}\left(\frac{Q_{channel}}{I_{channel}}\right)
\end{aligned}
\tag{4.3}
$$

The drive or summation signal of the gyroscope is represented as $A\sin(\omega t + \varphi)$ with φ being the phase difference. To achieve phase-lock, this phase output must remain constant which requires an adaptive PLL signal output to compensate for changes in the phase output.

4.4.2 Proportional-Integral Loop Filter

The loop filter used in this case is a PI filter, shown in Figure 23, to compensate for phase error with minimal steady-state error. The input to the PI filter is the difference between the CORDIC arctangent measurement and a phase setpoint measured at the resonant peak. When the difference between these phases is zero, the PI filter output does not change, but when the phase difference is non-zero, the PI filter outputs a value to add or subtract from the FTW value to redefine the sinusoidal signal frequency.

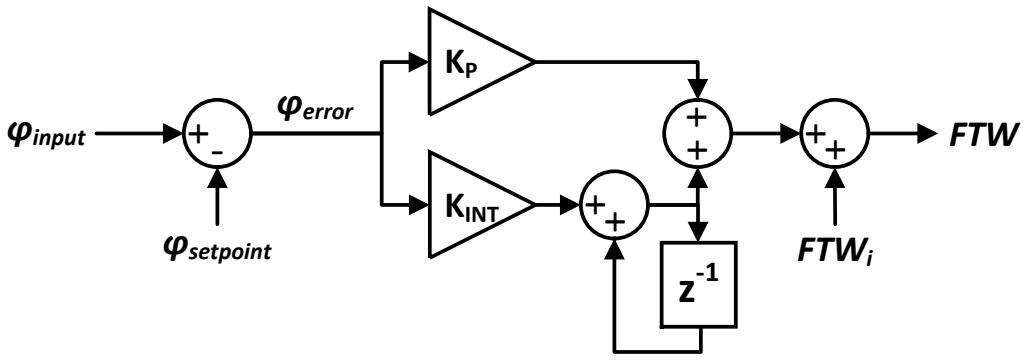


Figure 23 – Digital implementation of the PI filter used in the PLL to modify signal frequency based on phase error.

High-Q resonators are beneficial for good phase tracking as they allow for a sharp phase transition at the resonant peak of the device. Since a relatively large phase error is measured for a small deviation from resonant frequency, the resonant frequency can be effectively tracked to maintain phase-lock.

4.4.3 Numerically-Controlled Oscillator

The signal generation of a PLL is implemented through a numerically-controlled oscillator (NCO), shown in Figure 24. Similarly to the standard VCOs in analog PLLs, NCOs have an input that defines its frequency of operation. As mentioned in Section 4.3.1, DDS is implemented through use of a phase accumulator and CORDIC waveform generator, and the frequency is defined by the FTW of the phase accumulator [57], [58]. In this case, a 32-bit phase accumulator and 125 MHz clock frequency provides a frequency resolution of approximately 29.1 mHz to allow for the PLL to finely track the gyroscope resonant frequency as it drifts with time and temperature.

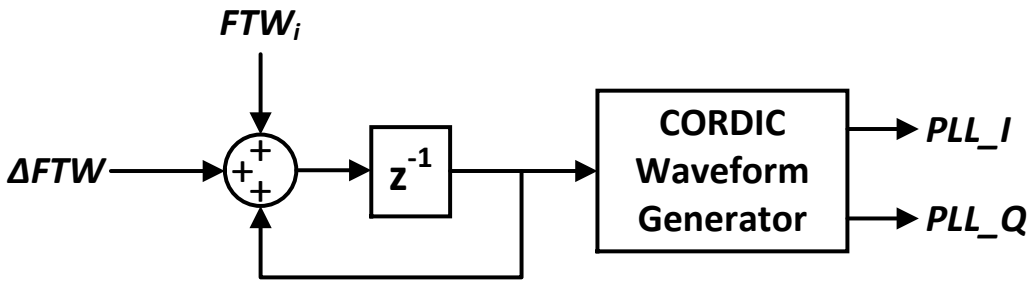


Figure 24 – CORDIC-based digital numerically-controlled oscillator that generates sine and cosine outputs.

4.5 Automatic Mode-Matching Loop

As detailed in Section 3.2.2, the quadrature-phase channel of the dual-mode difference output behaves as an indicator for mode split. This channel is decimated and filtered similarly to that of the rate output on the FPGA to be transferred to the RT controller without noise folding. The filtering of this mode-split indicator is different than that of the in-phase rate channel as it is related to the drifting apart of the gyroscopic modes across time and temperature which is a low-frequency operation. To reduce measurement noise as much as possible, a 2048-sample moving-average filter is used. The filtered output is the error signal for the automatic mode-matching control loop, implemented using a PI controller to add or subtract from an initial 16-bit word that defines the voltage output of the DAC that sets the tuning voltage. The 16-bit bias DAC voltage can be set in the range of 0 to 2.5 V to provide a voltage output resolution of approximately 38.1 μV, and an SPI engine was developed to periodically shift the updated voltage data to the DAC.

4.6 In-Run Scale Factor Calibration

Scale factor calibration is implemented by multiplying a digitally-generated waveform to the ADC output velocity signals. The resulting signals are then added to the actuation signals that are applied to the DACs. The digitally-generated virtual rate waveform, can be generated on the RT controller level due to its low frequency, which reduces the requirements of the FPGA. With a 10 kHz clock frequency, the virtual rate generator uses a phase accumulator similar to that of the CORDIC waveform to provide a frequency within the half-bandwidth of the gyro. From the RT controller, the signal is up-converted to a data rate of 125 MHz where it is multiplied by the feedback velocity signals from the gyro outputs of the ADCs. The resulting rate signals, containing the superposed virtual rate, follow the same signal chain as the physical rate, and once transmitted to the

RT controller, the same steps of the signal chain, mentioned in section 4.3.2, are followed as shown in Figure 25. This results in the superposition of a known virtual rate and an uncalibrated physical rate in the gyro output. To separate the two signals, the virtual rate is chosen to be a sinusoidal signal with a frequency that can be demodulated and filtered to provide a DC value that is proportional to the virtual rate amplitude. In the output channel for physical rate, the virtual stimulus is filtered out to provide only physical rate with no influence from the sinusoidal stimulus for scale factor calibration. While this scheme limits the measurement bandwidth, the resulting physical rate output is effectively scaled by the DC value extracted from the stimulus to provide a calibrated rate output.

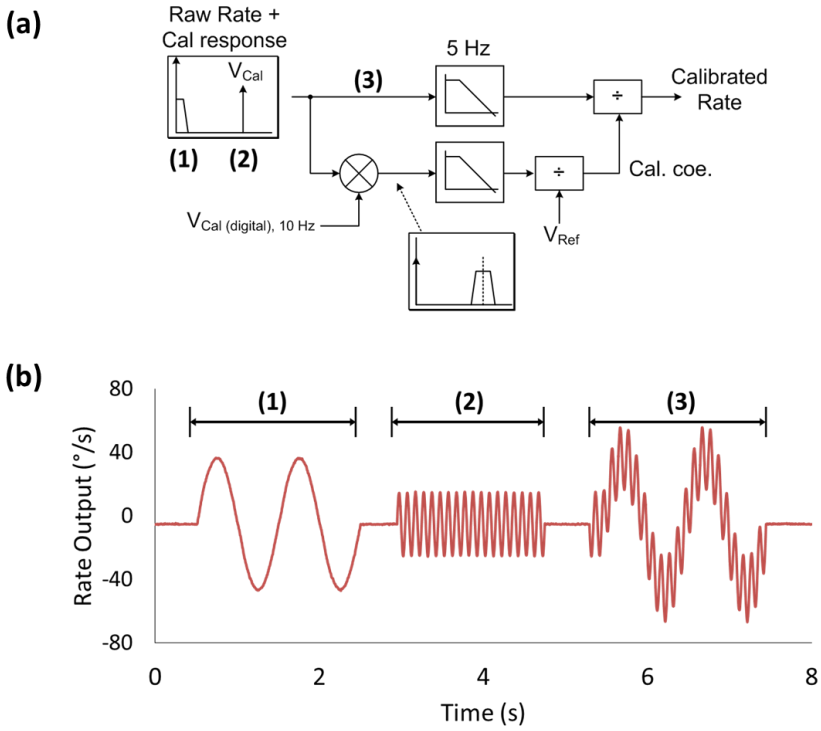


Figure 25 – (a) A band-limited scale factor calibration scheme to provide a calibrated rate output. (b) The measured physical rate (1), virtual rate (2), and combine physical and virtual rates (3).

CHAPTER 5: SYSTEM PERFORMANCE

A MEMS gyroscope digital interfacing architecture was implemented and evaluated using the National Instruments platform mentioned in Chapter 4 that contains a RT controller, an FPGA, and data converters to be interfaced with a host PC. The gyroscope was wirebonded to a custom PCB with input buffering amplifiers, output TIAs, difference amplifiers, and a 16-bit precision DAC. To evaluate the performance of the gyroscope with and without the calibration layers, the PCB signals were sent and received by the adapter module to convert the signals for digital communication and processing. By sweeping temperature from 15-85 °C, the performance is evaluated and compared to that of the conventional interfacing architecture. Single-DAC and dual-DAC configurations are used to demonstrate the influence of DAC noise in the rate output, and unless otherwise stated, the dual-DAC configuration should be assumed.

5.1 Experimental Setup

The first stage of the experimental setup is the PCB that provides a means for buffering actuation voltage, picking off output signals, converted from differential to single-ended signals, and applying bias voltages. The polarization voltage of 18 V and ±5 V supplies are provided with an Agilent triple output power supply (E3631A), and the bias voltages for frequency tuning and modal alignment are provided by a precision DAC from Texas Instruments (DAC8564). The NI 5782 adapter module also provides a means for controlling the bias DAC through use of its auxiliary I/O ports and an SPI engine implemented on the FPGA. Inverting amplifiers are used instead of voltage follower buffers to provide an option for amplitude scaling when a single DAC is used for signal

generation, and the purpose of single-DAC actuation is detailed more extensively in Section 5.3. Due to its high bandwidth and low noise, a dual amplifier from Analog Devices (AD8058) was used. The TIAs are used to amplify the output current signals and to convert them to voltages for the ADC inputs. To provide sufficient amplification while also providing a wide bandwidth for minimal attenuation and phase shift in the TIA outputs, OPA657 amplifiers from Texas Instruments were used with a 100 kΩ low-drift feedback resistor, and the board design is shown in Figure 26.

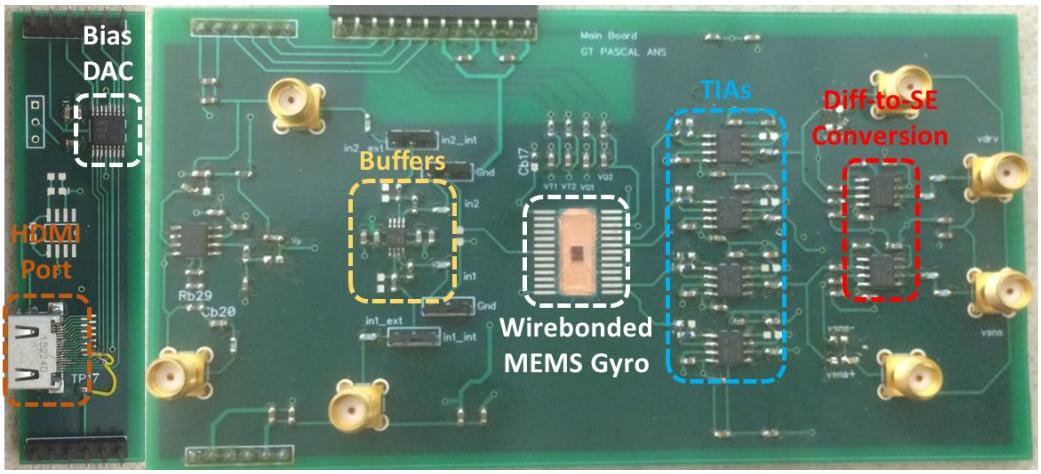


Figure 26 – PCBs with analog circuitry for gyro signal amplification and a bias DAC for tuning and alignment voltages.

The adapter module facilitates the drive and pick-off signal conversions, and the ADC outputs are processed by the NI PXIe-7961 FPGA board. The digital outputs of the FPGA are transferred through the backplane of a NI PXIe-1071 chassis and to the NI PXIe-8840 RT controller, where data can be further processed and acquired using either the open-loop or closed-loop user interfaces shown in Figures 27 and 28, respectively.

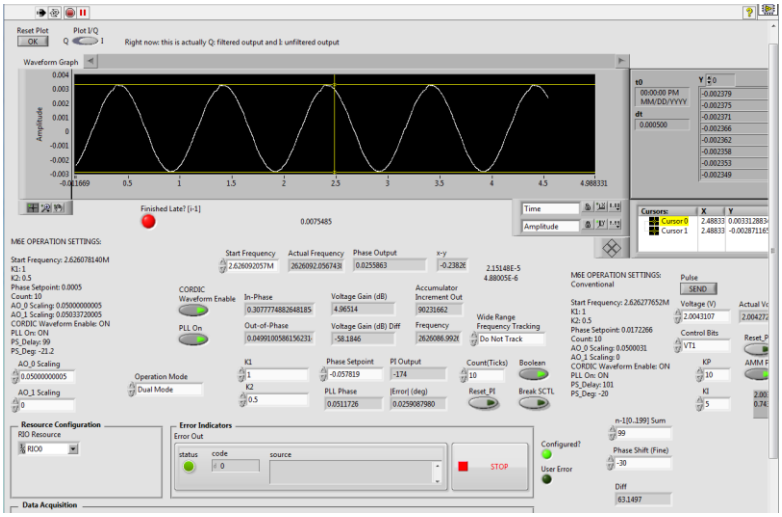


Figure 27 – Custom LabVIEW user interface for closed-loop rate readout.

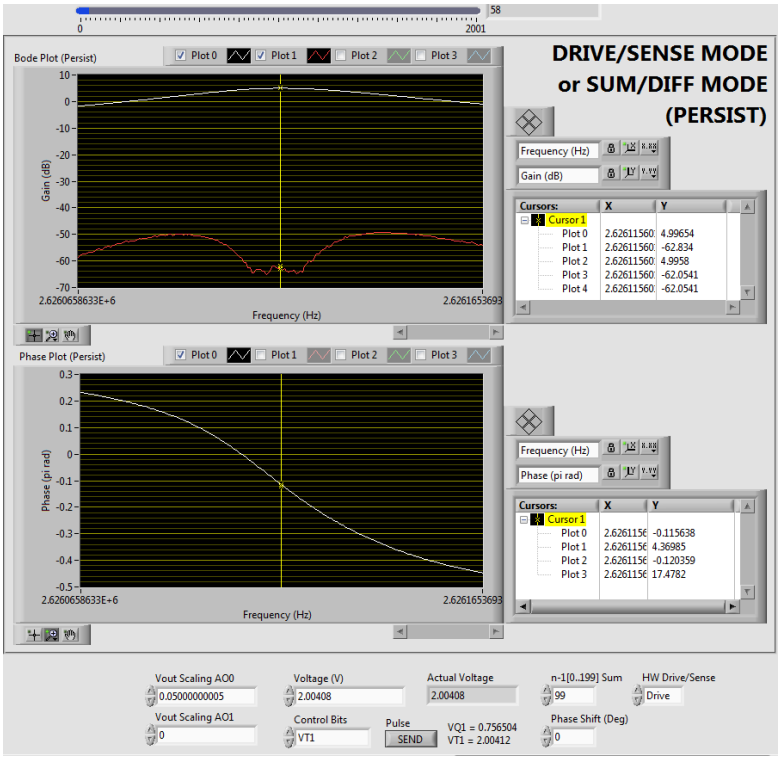


Figure 28 – Custom LabVIEW user interface for open-loop frequency sweep measurements.

To evaluate gyro performance, physical rate is applied and temperature is swept using an Ideal Aerosmith rate table (1291BR). Unless otherwise stated, physical scale factor

measurements are taken by analyzing the gyro response to a sinusoidal rate of 40 °/s at a frequency of 1 Hz. The full setup showing all components of the gyro system is shown in Figure 29.

Figure 29 – Experimental setup with the (a) Ideal Aerosmith rate table and (b) the power supplies, National Instruments setup, and PCB.

5.2 Measurement Methods

To analyze the performance of the gyroscope and the effectiveness of the calibration layers, measurement procedures were defined to provide a consistent way to evaluate system performance. The user interface allows for easy reconfigurability between single-mode and dual-mode architectures, and for dual-mode, dual-DAC or single-DAC actuation can be chosen with a simple PCB modification. The dual-DAC configuration uses both DAC outputs to drive the gyroscopic modes and enables scale factor calibration. The single-DAC configuration uses one DAC output to drive both modes of the gyro, but with this setup, the digital implementation of the scale factor calibration method is not possible. The following three procedures were primarily used for system measurements:

Allan variance analysis, temperature sweep measurements, and turn-on to turn-on repeatability measurements.

5.2.1 Allan Variance Analysis

Allan variance analysis is performed by acquiring data from the ZRO of the gyro to determine the noise and drift performance. Through the LabVIEW-based user interface, a text file is generated to store output data at a user-determined frequency of 2 kHz. Due to the simplicity of data acquisition, several hours of data can be taken at a time without consuming excessive storage space of the RT controller. The text file data is formatted to be compatible with Alavar, the software used to perform Allan variance analysis [59]. This software package allows for quick plotting of root Allan variance to characterize key gyro specifications such as ARW and bias instability.

5.2.2 Temperature Sweep Measurements

Since many of the errors induced in the gyroscope output are due to temperature fluctuations, sweeping the temperature provides valuable information to evaluate the effectiveness of bias and scale factor calibration. The temperature was swept from 15-85 °C in 10 °C increments with a settling period of 15-20 minutes at each point. Once the temperature is settled, data is acquired both with and without physical rate for 5 minutes each. To analyze the bias levels across temperature, the 5 minutes of ZRO data is averaged and plotted to show the bias drift across temperature. In Section 5.3, various conditions of measurements are shown to demonstrate the effectiveness of calibration layers such as architecture choice, automatic mode-matching, and insertion loss matching.

For accurate automatic mode-matching, it was found that gain and phase errors, induced by electronics, negatively affect performance. Gain and phase are compensated by characterizing the interface electronics with the major error contributors being the DACs, ADCs, and TIAs, and the errors are corrected by applying gains and phase shifts to the DAC inputs and demodulation signals. The following systems of equations can be used to characterize gain (A) and phase (θ) differences between each of the four data converters by connecting data converters directly:

$$\begin{matrix} A_{dB1} = A_{DAC0} + A_{ADC0} \\ A_{dB2} = A_{DAC0} + A_{ADC1} \\ A_{dB3} = A_{DAC1} + A_{ADC0} \\ A_{dB4} = A_{DAC1} + A_{ADC1} \end{matrix} \longrightarrow \begin{matrix} A_{dB1} - A_{dB3} = A_{DAC0} - A_{DAC1} \\ A_{dB2} - A_{dB4} = A_{DAC0} - A_{DAC1} \\ A_{dB1} - A_{dB2} = A_{ADC0} - A_{ADC1} \\ A_{dB3} - A_{dB4} = A_{ADC0} - A_{ADC1} \end{matrix} \tag{5.1}$$

$$\begin{matrix} \theta_{deg1} = \theta_{DAC0} + \theta_{ADC0} \\ \theta_{deg2} = \theta_{DAC0} + \theta_{ADC1} \\ \theta_{deg3} = \theta_{DAC1} + \theta_{ADC0} \\ \theta_{deg4} = \theta_{DAC1} + \theta_{ADC1} \end{matrix} \longrightarrow \begin{matrix} \theta_{deg1} - \theta_{deg3} = \theta_{DAC0} - \theta_{DAC1} \\ \theta_{deg1} - \theta_{deg3} = \theta_{DAC0} - \theta_{DAC1} \\ \theta_{deg1} - \theta_{deg3} = \theta_{ADC0} - \theta_{ADC1} \\ \theta_{deg1} - \theta_{deg3} = \theta_{ADC0} - \theta_{ADC1} \end{matrix} \tag{5.2}$$

It is shown that there are two results given for each resulting difference of gain and phase between DACs and ADCs. Each similar result should have near equal values with only slight measurement error, and if the results are significantly different, they serve as an error check. Measurements are to be taken and corrected iteratively until the errors are sufficiently minimized. Phase and gain errors are also apparent in the TIA outputs. Due to mismatches between the multiple TIAs and feedback resistors, the gain and phase responses are not equal. These errors can be compensated by shifting and scaling the demodulation signals. Finally, the last layer of phase compensation corrects for the phase error change across frequency. The phase shift of the data converters changes linearly

across frequency, and the resonant frequency changes across temperature. Therefore, when sweeping temperature, phase error is apparent in the output which induces error in the lock-in phase. This causes the gyro to be driven at a frequency slightly offset from the resonant frequency for closed-loop measurements resulting in errant conditions for rate readout.

To analyze scale factor drift, physical rate is applied to collect rate output data for 5 minutes, and peak-to-peak analysis can be averaged over the time duration of the measurement. While no form of in-run scale factor calibration is implemented for conventional gyro operation, the dual-mode architecture scale factor calibration is enabled to give a side-by-side comparison of single-mode and dual-mode scale factor drift.

5.2.3 Turn-on to Turn-on Repeatability Measurements

Another way to evaluate the robustness of the in-run calibration layers is through use of turn-on to turn-on measurements. For these measurements, the supply voltages of the gyro are turned off and on forcing the gyro to cool down and heat up repeatedly. While LUT-based approaches rely on similar gyro behavior through each measurement cycle, the in-run self-calibration techniques of the dual-mode architecture essentially track the mechanical error contributors for bias and scale factor drift making it a more robust means for compensation. The bias repeatability is compared to an initial baseline measurement and measured with respect the full-scale range of the gyroscope in ppmFS (parts-per-million full-scale). The full-scale range is determined by the half-bandwidth of the gyro to be ~10,000 °/s. For each measurement, the settling time after turn-on is 30 minutes, and ZRO and sinusoidal rate data is acquired for 5 minutes each. For scale factor repeatability,

the physical and virtual calibration stimuli are analyzed by taking an FFT of acquired data from the rate output.

5.3 Experimental Results

While this implementation of the dual-mode architecture does not reach the ultimate goal of 1 ppm turn-on to turn-on repeatability of bias and scale factor, it demonstrates the effectiveness of the dual-mode calibration layers and sets the stage for future incremental improvements to achieve the target specifications. This section reports the results of the digital architecture, and the residual errors are further discussed in the next chapter.

5.3.1 Allan Variance Analysis

Due to the reduction in bias terms and increased scale factor of the dual-mode architecture, the bias instability and ARW have shown to be reduced when compared to the conventional architecture. The bias instability is affected by the method of applying actuation voltage of the gyroscopic modes. Using the dual-DAC architecture significantly degrades the bias instability of the gyro, and it is shown that with the single-DAC configuration the bias instability can be reduced to a similar level to that of single-mode. The noise reduction with the single-DAC configuration is due to the correlation of close-in flicker noise at carrier of single-DAC. Since the noise in this case is correlated, the noise is mostly canceled in the difference output. The dual-DAC configuration produces uncorrelated close-in flicker noise in each channel to increase the total noise in the difference output of the dual-mode architecture, and the Allan variance plot showing the conventional and dual-mode performance is given in Figure 30.

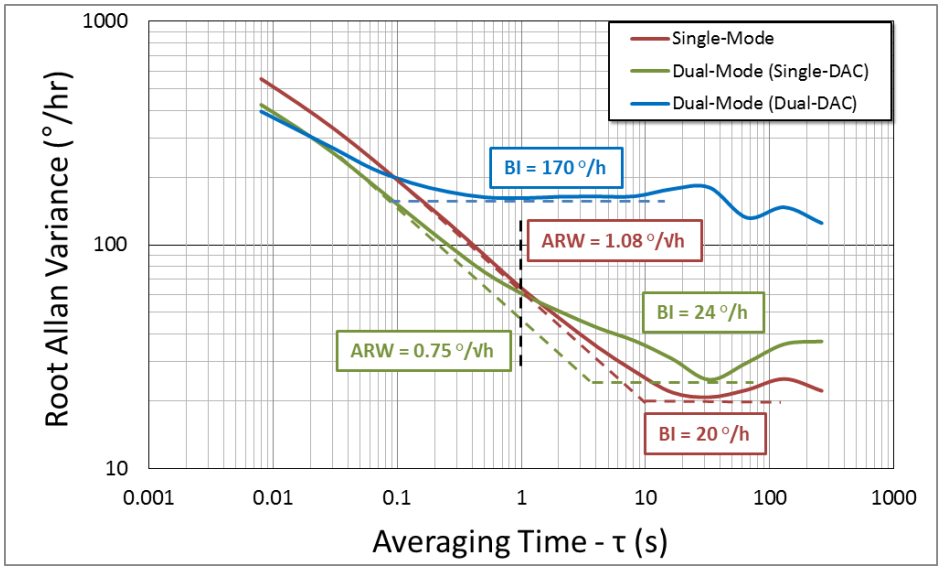


Figure 30 - Allan variance measurements showing long-term bias drift measurements.

It is shown that for both DAC configurations in dual-mode, the ARW of dual-mode (0.75 °/√h) is improved ~1.4 times compared to that of the conventional architecture (1.08 °/√h), and due to the noise correlation of single-DAC actuation, the bias instability of dual-mode (24 °/h) has shown to be close to that of conventional operation (21 °/h). With this method, scaling of the actuation signals is done by adjusting resistors. While single-DAC actuation cannot replace dual-DAC actuation for full implementation of digital scale factor calibration, it clearly illustrates that the degraded bias instability (170 °/h) is due to the actuation signal noise, and this noise will be further discussed in Chapter 6.

5.3.2 Temperature Sweep Measurements

Temperature was swept from 15-85 °C to evaluate the effectiveness of the calibration layers described in this thesis. Various system enhancements were made to the dual-mode implementation to improve bias drift across temperature such as automatic

mode-matching, insertion loss matching, and gain/phase compensation. The effectiveness of scale factor calibration is heavily dependent on the frequency of the virtual stimulus. Since the quality factor determines the scale factor of a gyro at a certain frequency, a given harmonic may change slightly differently for high-Q gyroscopes. This has been noticed through the use of different virtual rate frequencies where the virtual stimulus was used to calibrate physical rate across temperature.

5.3.2.1 Bias Drift over Temperature

The bias drift performance is evaluated by sweeping temperature to compare uncalibrated single-mode and calibrated dual-mode performance, and a comparison of various layers of calibration is shown as well. The data converter and TIA errors in phase and gain, as detailed in the previous section, were compensated, and the error values are shown in Table 2.

Table 2 – Results from electronic error measurements

Error Measurement	Gain Error (dB)	Phase Error (°)	Phase Drift (°/kHz)
$\mathbf{DAC_0 - DAC_1}$	-0.01917	-0.08121	N/A
$\mathbf{ADC_0 - ADC_1}$	-0.00104	0.57804	N/A
$\mathbf{TIA_{diff,0} - TIA_{diff,1}}$	-0.00126	-0.52798	N/A
$\mathbf{DAC_0 + ADC_0}$	N/A	N/A	0.17266
$\mathbf{DAC_1 + ADC_1}$	N/A	N/A	0.17104

Using automatic mode-matching and gain/phase compensation for the dual-mode configuration, the bias drift shows over 20x improvement to single-mode when using gain/phase compensation with automatic mode-matching as shown in Figure 31.

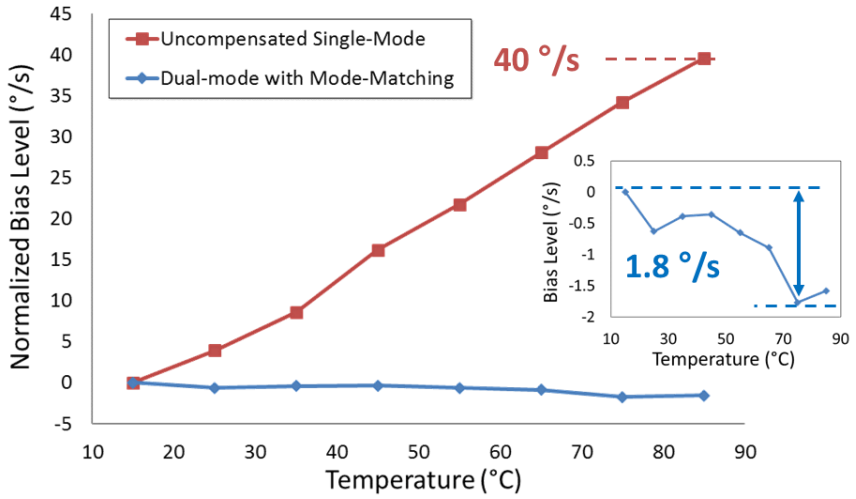


Figure 31 – Comparison of single-mode and dual-mode bias drift measurements over temperature

The effectiveness of the individual calibration layers are contrasted in Figure 32.

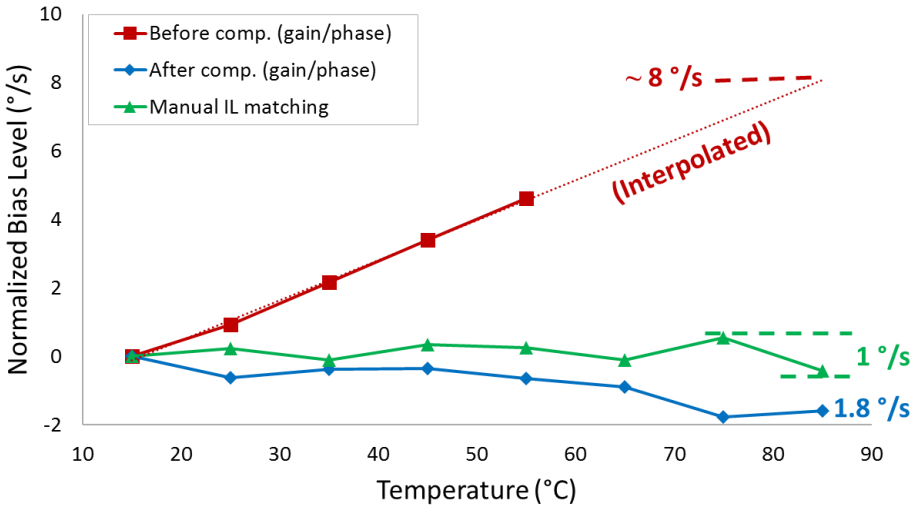


Figure 32 – Improvements in bias drift across temperature with various layers of compensation using the dual-mode architecture with automatic mode-matching

In the figure shown above, three cases are observed to investigate the effect of various calibration layers with the dual-mode architecture. Before phase and gain compensation was implemented, the temperature was swept from 15-55 °C with automatic mode-matching in place to show a drift of ~4.6 °/s, and with the assumption that the linear trend remains consistent, the drift is ~8 °/s between 15-85 °C. With no compensation for electronic-induced gain and phase errors, the mechanical characteristics are essentially masked to result in increased drift, and with these compensation measures in place, the drift is reduced by over 4x to be ~1.8 °/s. It is also shown that with manual matching of IL between the two modes, the drift can be further reduced, and with a closed-loop IL-matching scheme, the drift is likely to be significantly further reduced.

5.3.2.2 Scale Factor Drift over Temperature

The results shown in this section compare the performance of the calibrated dual-mode architecture to that of the uncalibrated single-mode architecture. Two different scale factor drift measurements are shown for calibrated dual-mode. One case uses a 25 Hz virtual stimulus, and the other uses a 10 Hz stimulus. Since the physical stimulus, used in these measurements has a 1 Hz frequency, the 10 Hz stimulus provides superior drift performance across temperature compared to that of the 25 Hz stimulus or uncalibrated single-mode, and the results are shown in Figure 33. The scale factor drift of dual-mode with the 10 Hz stimulus gives a scale factor drift of 1.1% across the temperature range, which is over 50x improvement compared to the uncalibrated single-mode drift of 57.5% over temperature. Using a 25 Hz stimulus gave a drift of 12.3 which showed improvement compared to uncalibrated single-mode but did not perform to the level of the 10 Hz stimulus measurement.

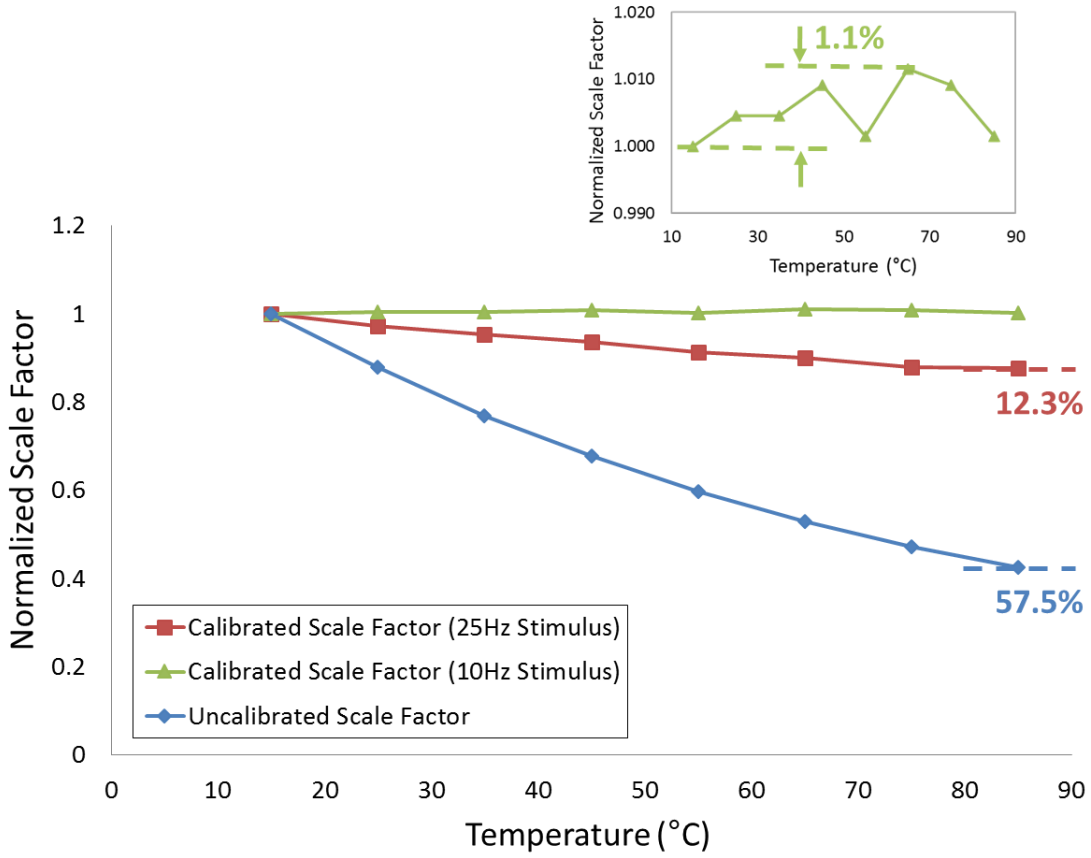


Figure 33 - Comparison of scale factor drift between single-mode and dual-mode architectures

5.3.3 Turn-on to Turn-on Repeatability Measurements

By power cycling the device, the performance can be evaluated by measuring the drift from turn-on to turn-on. For each measurement run, there is a 30 minute wait time before the single-mode and dual-mode measurements are taken for bias and scale factor, and the measurements are shown in Figures 34 and 35. Turn-on to turn-on bias repeatability has shown to be improved by over 4x. This was accomplished with the single-DAC configuration to keep the flicker noise low. With low noise, the repeatability gives its best performance due to the decreased drift. For clarity, it should be noted that the dual-DAC configuration was used for scale factor measurements.

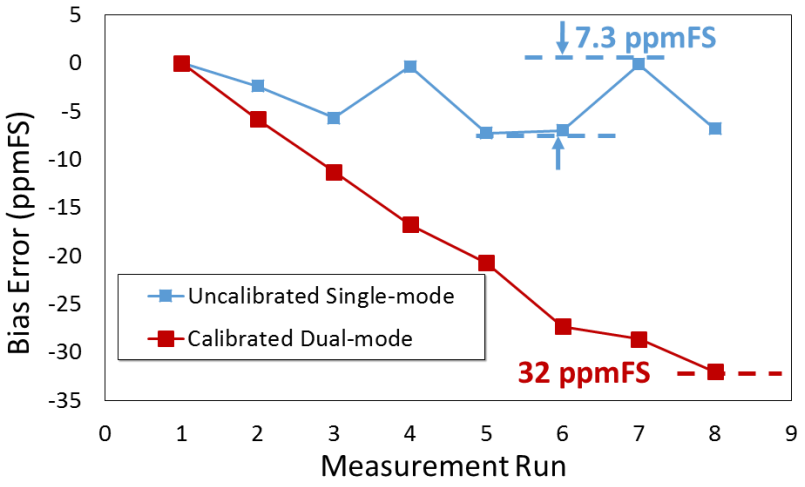


Figure 34 – Turn-on to turn-on repeatability measurements of bias error for single-mode and dual-mode with single-DAC configuration.

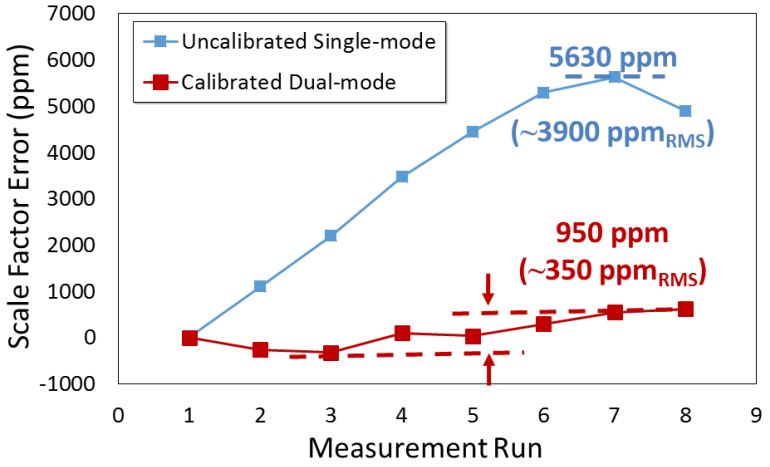


Figure 35 - Turn-on to turn-on repeatability measurements of scale factor error for single-mode and dual-mode.

While the accuracy of scale factor repeatability measurements depends on the drift performance, significant improvement can be shown between uncalibrated single-mode and calibrated dual-mode. Dual-mode shows an improvement of over 10x from RMS measurements of scale factor repeatability, and with reduced noise from the actuation signal generation, the performance can be further improved.

CHAPTER 6: CONCLUSION AND FUTURE WORK

While the presented implementation of a digital gyro interfacing architecture has made great strides in providing in-run gyro self-calibration, some remaining error sources contribute to the overall drift of the gyro. One such contributor is the noisy outputs of the current-steering DACs that degrade the bias instability of the gyro. It is also apparent that some additional calibration layers, to compensate for the changes in mechanical bandwidth and capacitive gap variations, will be necessary. The error sources are further detailed in this chapter along with potential solutions.

6.1 Remaining Error Sources

The most significant contributor to gyro errors is the close-in flicker noise of the actuation signals generated from the current-steering DACs. This degrades the bias instability of the gyro and increases uncertainty in the scale factor repeatability measurements. Another source of error is the apparent insertion loss variations across temperature. To decrease the temperature-induced bias drift, the insertion loss of each mode must maintain the same level across time and temperature, and to decrease the effective scale factor drift, the changes observed in the virtual calibration stimulus must be representative of the changes in physical rate.

6.1.1 Current-Steering DAC Flicker Noise

Flicker noise of the DC current sources is up-converted to the carrier frequency in current steering DACs [60], the most commonly used consumer DACs for high-frequency data conversion. Since most low-frequency gyroscopes operate at lower frequencies, other

DAC architectures are able to be used in the system, but high-frequency gyroscopes are primarily restricted to using current-steering DACs. It is shown below that current noise power ($I_{1/f}^2$) increases with increasing current levels due to the increased transconductance (g_m) of the switching DAC current sources:

$$\overline{I_{1/f}^{\,2}} = g_m^{\,2} \frac{K_{1/f}}{WLC_{ox}} \frac{1}{f} \tag{6.1}$$

In this relationship, flicker noise is also related to the process-related constant ($K_{1/f}$), transistor length (L), transistor width (W), oxide capacitance (C_{ox}), and frequency offset from DC (f). The periodic switching of current sources up-converts the flicker noise to the frequency of the sinusoidal output, and the result is a harmonic with a 1/f noise profile as demonstrated by Figure 36.

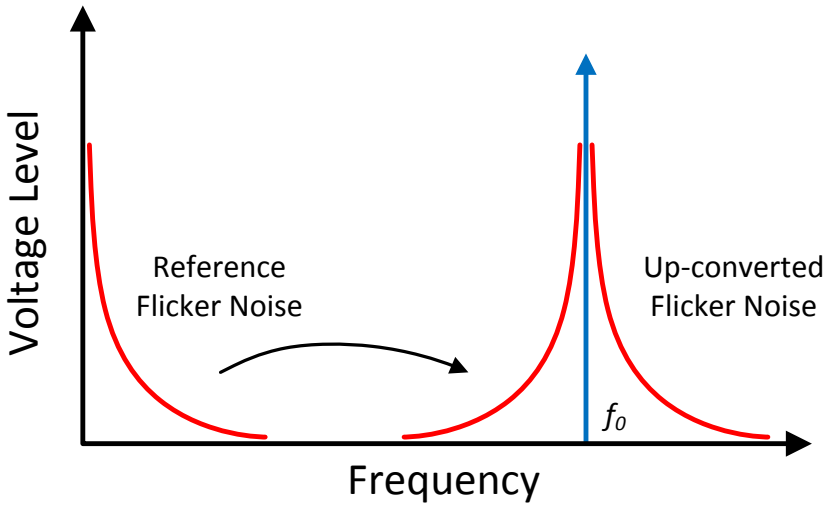


Figure 36 – Illustration showing the up-conversion of reference flicker noise to that of the carrier frequency.

Allan deviation measurements were taken to help verify the flicker noise profile of demodulated signals that were generated by the current-steering DACs, received by the ADCs, and processed with a similar signal chain to that of the gyro signals. These measurement results are shown in Figure 37.

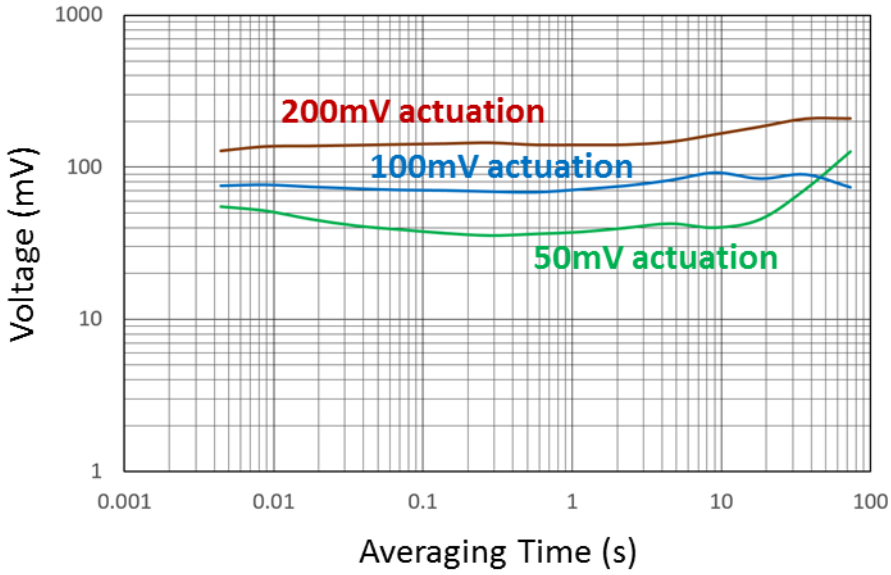


Figure 37 – Measurements supporting the fact that the level of flicker noise increases along with waveform amplitude.

Characterized by a flat profile in Allan deviation measurements, flicker noise is shown to be present in the demodulated signals, and the increase in flicker with amplitude verifies that flicker noise is indeed up-converted to the frequency of the carrier signal.

6.1.2 Scale Factor Measurement Uncertainty

With a relatively high bias instability in the gyro output for the dual-mode architecture, the scale factor measurement uncertainty is determined by the physical rate being applied. Since the application of physical rate is limited due to wire and cable

connections from the current experimental setup to the rate table, the rate amplitude is limited by cable stress. For the measurements that were shown in Figure 36, a rate amplitude of ~100 °/s was used to minimize the uncertainty to approximately 470 ppm_{RMS}. This is a simple estimation that results from dividing the dual-mode bias instability of 170 °/h (0.047 °/s) by the applied physical rate of 100 °/s, and the overall variation of the scale factor measurement uncertainty is comparable to the root-mean-square scale factor repeatability of ~350 ppm_{RMS} shown by the repeatability measurements. By improving the noise performance of the current-steering DACs or increasing the applied physical rate, the reliability of scale factor repeatability measurements can be improved.

6.1.3 Bias Drift from Insertion Loss Mismatch

The temperature sweep measurements, shown in Figure 32, illustrate the effect that IL-mismatch has on the bias drift. The best result for bias drift across temperature (~1 °/s at 15-85 °C) was measured when the insertion losses of each mode were manually adjusted to be equal at each temperature point by modifying the actuation voltages. Due to the time duration between the open-loop IL and closed-loop bias measurements, it is likely that there is some mismatch exhibited due to temperature variation, and with a closed-loop method for IL-matching there is potential for further improvement in performance. The two primary drift-inducing parameters that influence insertion loss are quality factor and transduction coefficient, and efforts are being made to implement in-run tracking of these parameters. Details of a potential architecture are given in future work.

6.1.4 Scale Factor Drift from Bandwidth Variations

It has been shown in Figure 33 that the use of a virtual calibration stimulus can reduce scale factor drift across temperature. The stimulus can be designed to fit the extraction method. In the measurements presented in this thesis, sinusoidal tones with frequencies of 25 Hz and 10 Hz were used, and it was shown that the 10 Hz stimulus gives better improvement in scale factor drift than that of the 25 Hz stimulus by using a simple extraction method that limits the measurement bandwidth of the physical rate output. As illustrated by Figure 38, the mechanical bandwidth changes due to quality factor and frequency drift across temperature, and these changes induce a variable proportionality between the physical rate magnitude and virtual rate magnitude.

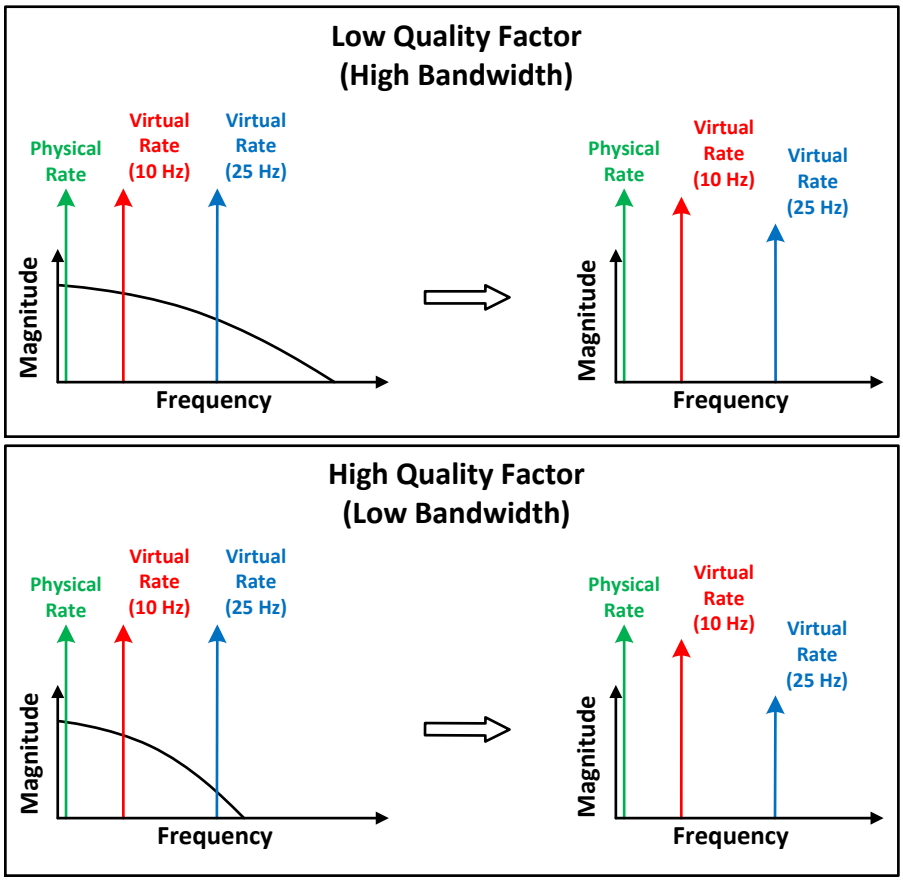


Figure 38 – Illustration of physical rate and virtual rate magnitude differences between low quality factor and high quality factor responses.

6.2 Future Work

For future improvements to this implementation will need to address the issues related to bias instability, bias and scale factor repeatability, and bias and scale factor drift across temperature. The most pressing improvement needed for high-grade gyro performance is the implementation of a low-noise DAC to mitigate the errors related to the high bias instability present in the dual-mode architecture. The increased bias stability also reduces the precision of bias and scale factor repeatability measurements. Drift of bias and scale factor across temperature is another issue that must be addressed, and description of future work to be done to solve these issues is shown in the following subsections.

6.2.1 Bias Instability Reduction

As previously mentioned, current-steering DACs are the most prominent consumer DACs able to generate signals at the BAW gyro's operating frequency. One alternative DAC architecture that can be used in this case is a bandpass sigma-delta (BP-ΣΔ) that has a bandpass characteristic centered about the operating frequency of the gyro as shown in Figure 39.

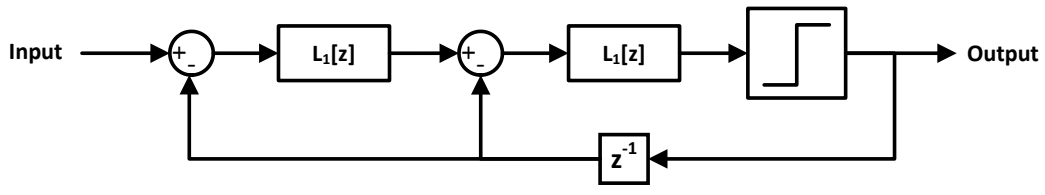


Figure 39 – Bandpass ΣΔ DAC architecture implemented on the FPGA

Since the quantization noise of a BP-ΣΔ is shaped to exist outside of the band of interest, high data rates are not needed to spread the noise power across the spectrum [61]. In this

case, Figure 40 shows that the BP-ΣΔ can be implemented on the FPGA to output a bit-stream of the noise-shaped signal.

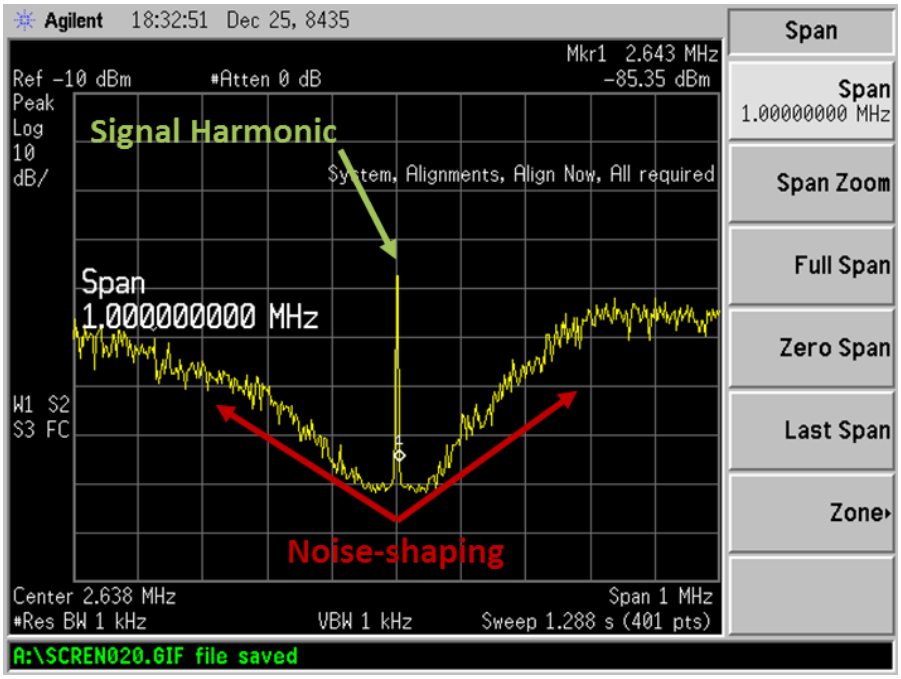


Figure 40 – Spectrum analyzer display showing the measured noise-shaping characteristics of the BP- ΣΔ architecture.

The noise-shaping capabilities of the BP-ΣΔ have been successfully demonstrated, but to be practical for signal-generation, the white noise from the voltage reference must be reduced as much as possible to prevent excessive white noise in the output. The low-noise implementation of the BP-ΣΔ is an ongoing effort, and once it is successfully realized, the level of bias instability will be reduced to provide improved bias and scale factor repeatability.

6.2.2 High-Precision Scale Factor Measurements

Scale factor repeatability can also be improved by modifying the measurement scheme to allow for DC rotation. With constant high-speed rotation, the noise in the rate

output can be averaged more effectively to increase measurement precision. The current setup does not allow for high-speed DC rotations since the power supply and signal cables are needed to measure physical rate, but by using low-noise slip-ring connections, the measurement capabilities of scale factor stability will allow the use of high rate application for longer periods of time. A low-noise slip-ring setup is currently under development.

6.2.3 Temperature-Related Drift Improvements

To provide in-run IL-matching capabilities, drift of the transduction coefficients (η) is the most notable contributor to the mismatch, and change in the difference between quality factors (ΔQ) of each mode induces IL-mismatch as well. A preliminary architecture has been developed to track the η drift across temperature as shown in Figure 41, but the data converter configuration does not facilitate the full implementation of this architecture.

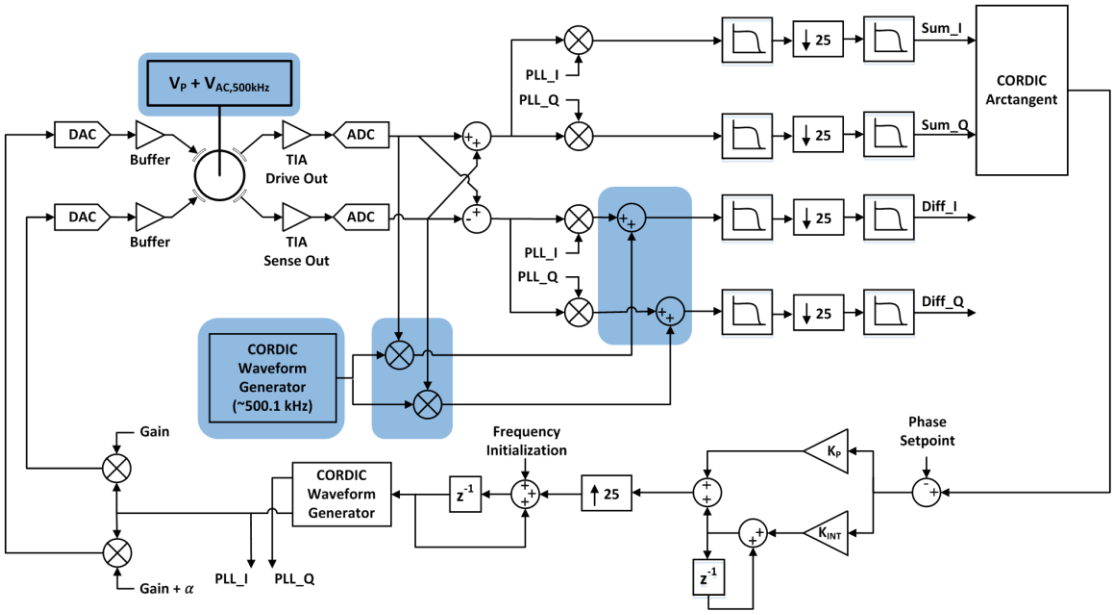


Figure 41 – Digital implementation of the dual-mode architecture with the highlighted additions for η characterization.

It is shown that the architecture uses an off-resonant signal applied as an offset to the polarization voltage. To share a common digital signal chain with the other gyro outputs, the off-resonant signal is down-converted to a frequency of 100 Hz, and the resulting signals are added to the signal chains before the first stage of filtering. On the RT controller level, the 100 Hz signal does not affect the rate output, and the amplitude exhibits change related to drifts in η. While the signal was able to be track changes in the capacitive gap, a closed-loop implementation cannot yet be achieved without additional data converters. In-run Q characterization is also necessary if ΔQ cannot be assumed to remain constant over temperature. It has been demonstrated that for substrate-decoupled BAW gyros, the ΔQ remains fairly constant over temperature making them the lesser contributor to IL-mismatch in this case, but for a more universal implementation of this architecture, a Q-tracking scheme would be necessary.

Another motivation to reduce scale factor drift across temperature is to implement a pattern of signals that is distinguishable from physical rate to provide more accurate calibration without band-limiting the output. To extract the information necessary for scale factor calibration, the signal pattern will be characterized to determine the behavior of virtual rate at higher frequencies that are close to the edge of the passband, and the data extracted for multiple higher virtual rate frequencies will be used to interpolate the response for lower frequencies.

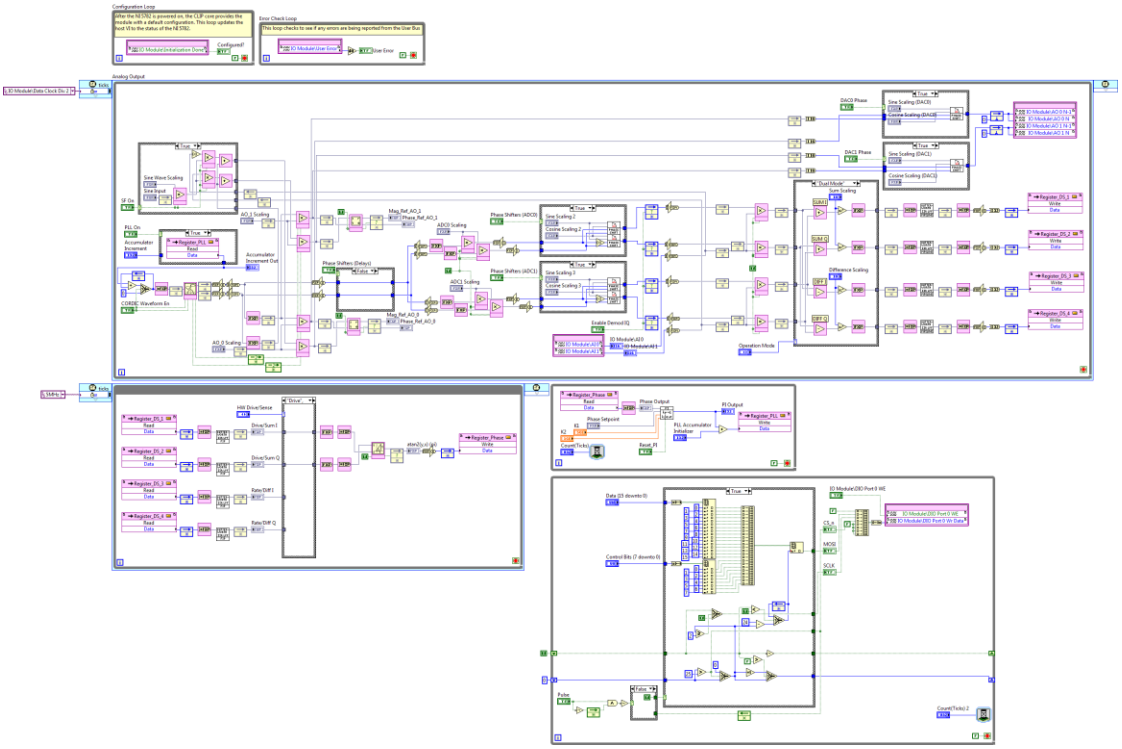
6.2.4 Standalone FPGA System Development

Finally, for this architecture to be used on virtually any practical platform, a stand-alone system will need to be developed. To accomplish this task, the LabVIEW-based

FPGA block diagrams will need to be translated to an HDL language such as VHDL or Verilog to program a standalone FPGA. The FPGA will allow for the programmability of all high-speed functions currently being executed on the National Instruments setup, and a microprocessor will be used to execute the RT controller functions. Data converters will be implemented to facilitate communication between the FPGA and gyro board, and once this generation of the system is developed, an ASIC containing the analog and digital functions will be the final step to provide a deliverable product.

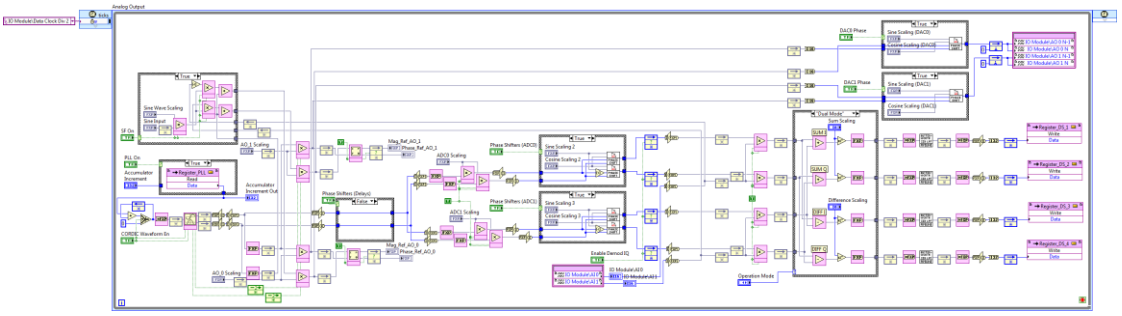
APPENDIX A. LABVIEW BLOCK DIAGRAMS

A.1 LabVIEW FPGA Block Diagram – Top Level VI



- Illustration of block diagram for all FPGA-based digital signal processes

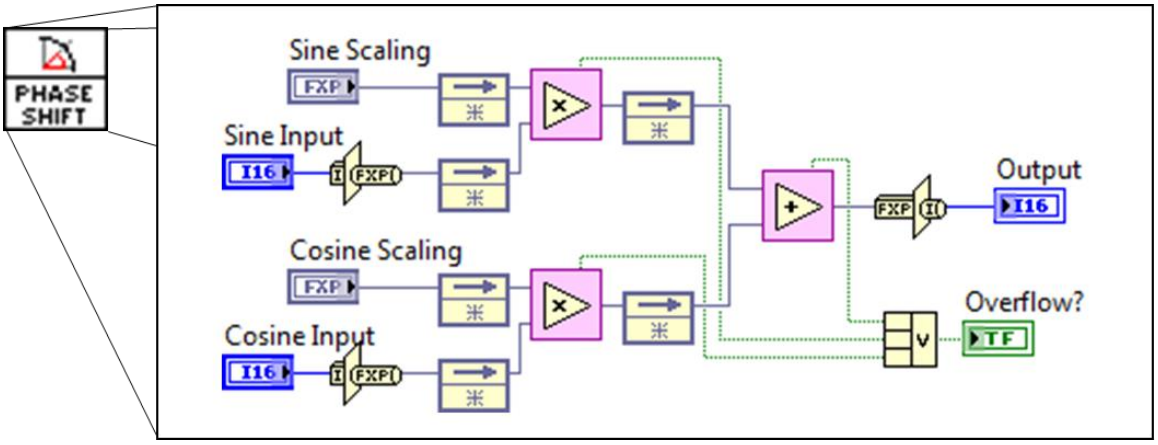
A.1.1 LabVIEW FPGA Block Diagram – 125 MHz SCTL



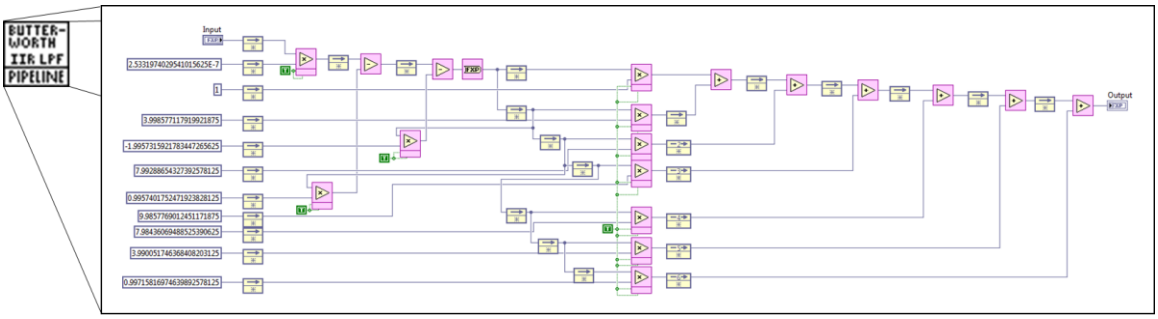
- A/D and D/A interfaces

- Sinusoidal waveform generation with CORDIC block and phase accumulator
- Voltage scaling of sinusoidal waveforms
- Scale factor calibration stimulus multiplication with velocity feedback with the result being added to the DAC input signal
- Phase shifters for compensation of gain/phase errors of data converters and digital electronics
- Signal demodulation and pipelined IIR low-pass filter implementation (1st stage)
- Switchable single-mode and dual-mode operation

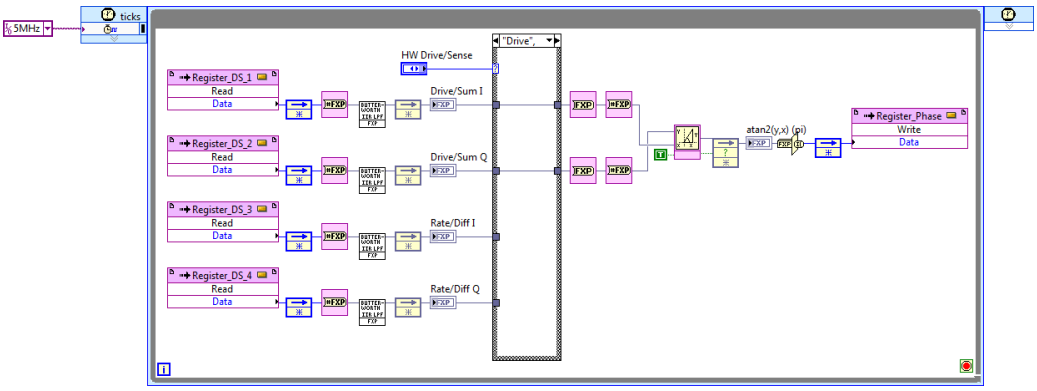
A.1.1.1 Sub VI – Pipelined IIR Butterworth Filter



A.1.1.2 Sub VI – Phase Shifter

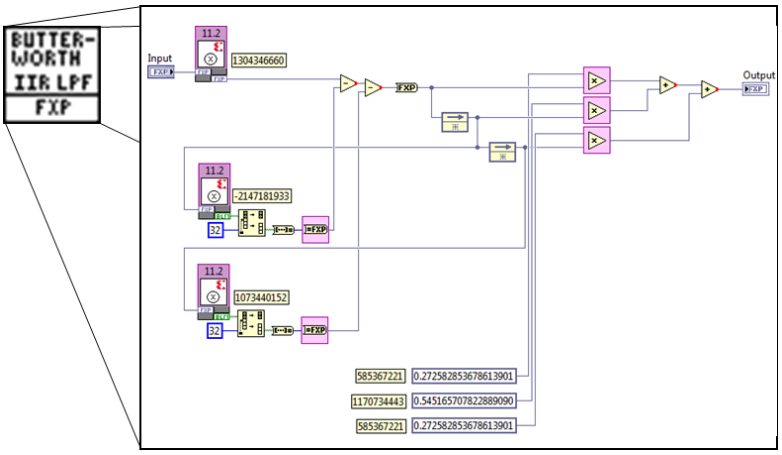


A.1.2 LabVIEW FPGA Block Diagram – 5 MHz SCTL

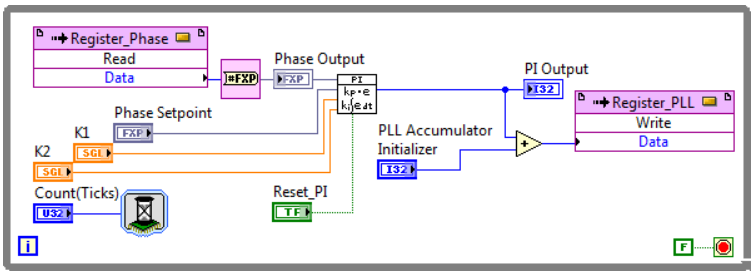


- IIR filter implementation (2nd stage)
- CORDIC arctangent calculation for PLL operation

A.1.2.1 Sub VI – IIR Butterworth Filter

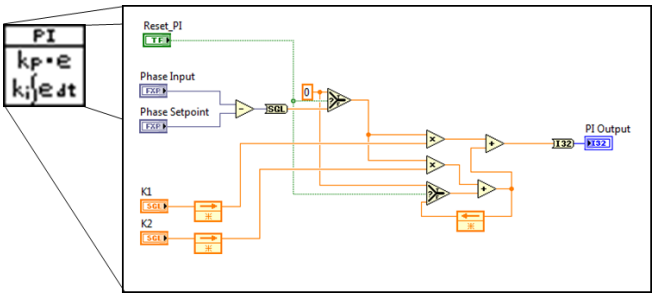


A.1.3 LabVIEW FPGA Block Diagram – PI Filter While Loop

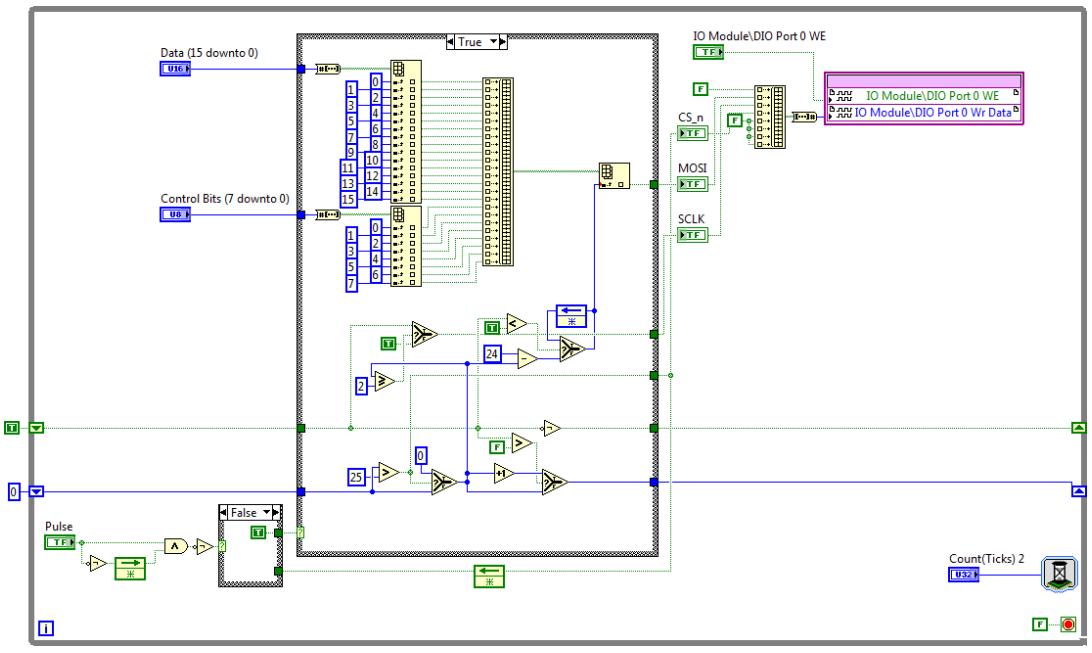


- PI filter implementation for closed-loop PLL operation
- Reconfigurable inputs for filter parameters (K1 and K2)
- Minimization of phase error (phase output – phase setpoint) for automatic signal frequency adjustments

A.1.3.1 Sub VI – PI Filter

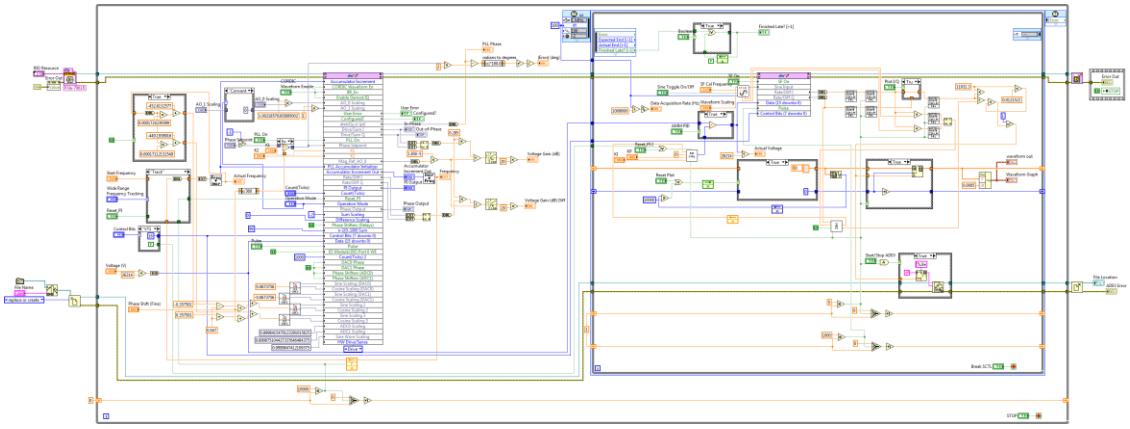


A.1.4 LabVIEW FPGA Block Diagram – SPI Engine



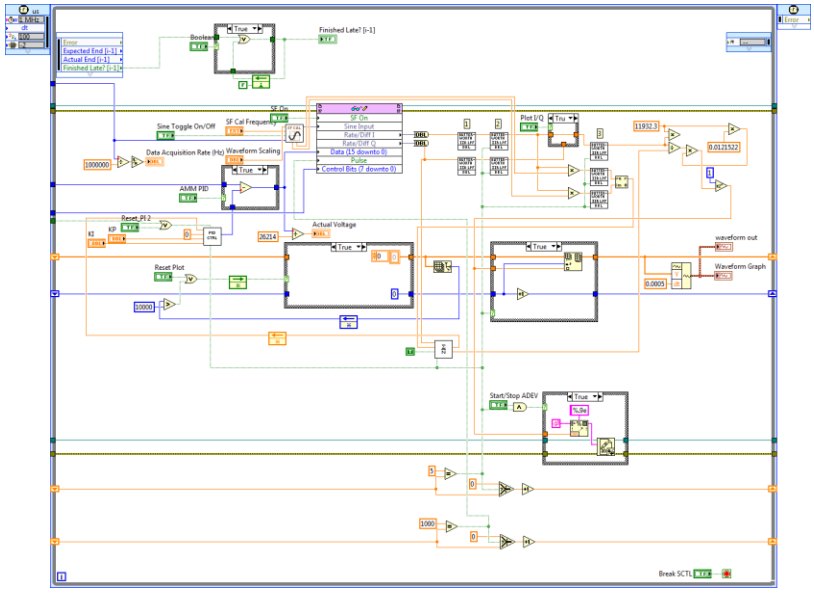
- Custom SPI engine for communication with bias DACs
- Configurable for periodic or manual voltage data updates

A.2 LabVIEW RT Controller Block Diagram – Top Level VI



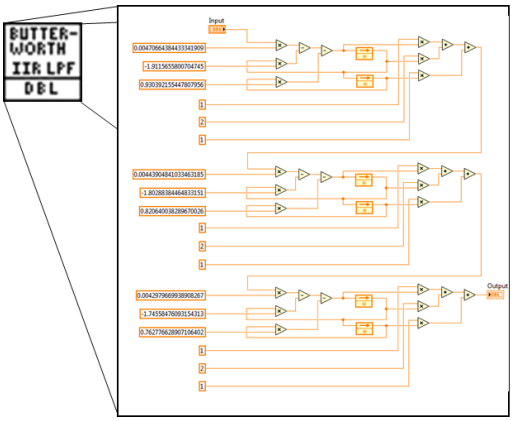
- Communication and mathematical calculations between user settings and FPGA I/O
- Separation between time-sensitive and not time-sensitive processes with glitch indicator

A.2.1 LabVIEW RT Block Diagram – 10 kHz SCTL Section



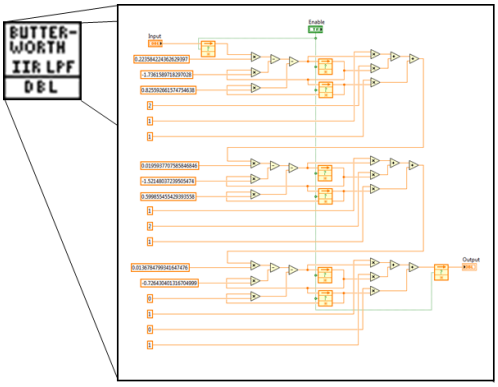
- Text file generation and writing for 2 kHz data acquisition enabling Allan variance measurements
- IIR filter implementation (3rd stage, 4th stage, and 5th stage)
- Automatic mode-matching PI filter to modify voltages based on a moving-average filtered mode-split indicator output
- Signal generation for virtual stimulus used to implement scale factor calibration
- Plot generation for a real-time rate readout display

A.2.1.1 Sub VI – 3rd Stage IIR Filter



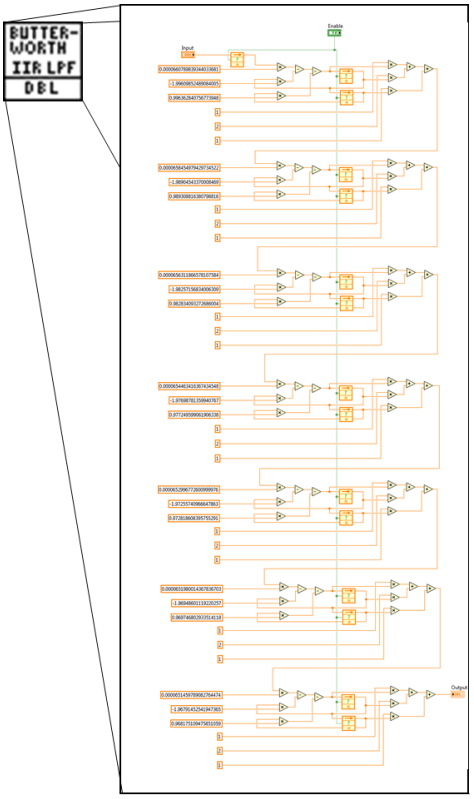
f_s = 10 kHz; $f_{passband}$ = 200 Hz; $f_{stopband}$ = 1000 Hz
$A_{passband}$ = -3 dB; $A_{stopband}$ = -80 dB

A.2.1.2 Sub VI – 4th Stage IIR Filter



f_s = 2 kHz; $f_{passband}$ = 100 Hz; $f_{stopband}$ = 500 Hz
$A_{passband}$ = -3 dB; $A_{stopband}$ = -80 dB

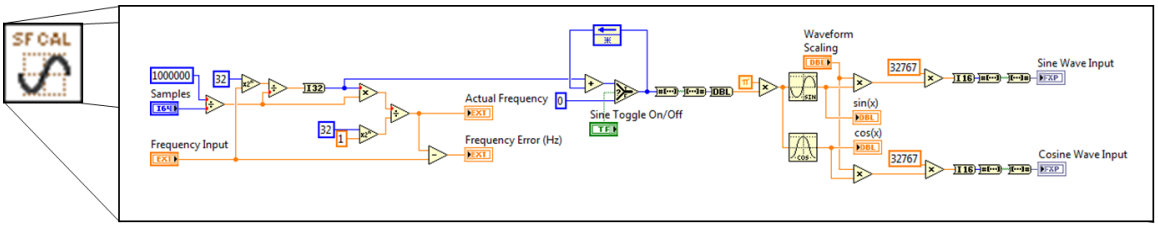
A.2.1.3 Sub VI – 5th Stage IIR Filter



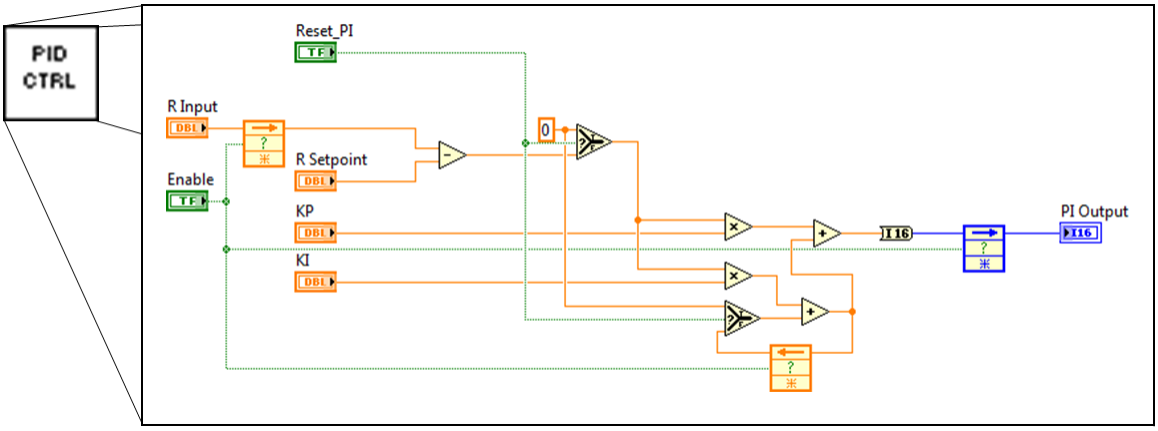
f_s = 2 kHz; $f_{passband}$ = 5 Hz; $f_{stopband}$ = 10 Hz

$A_{passband}$ = -3 dB; $A_{stopband}$ = -80 dB

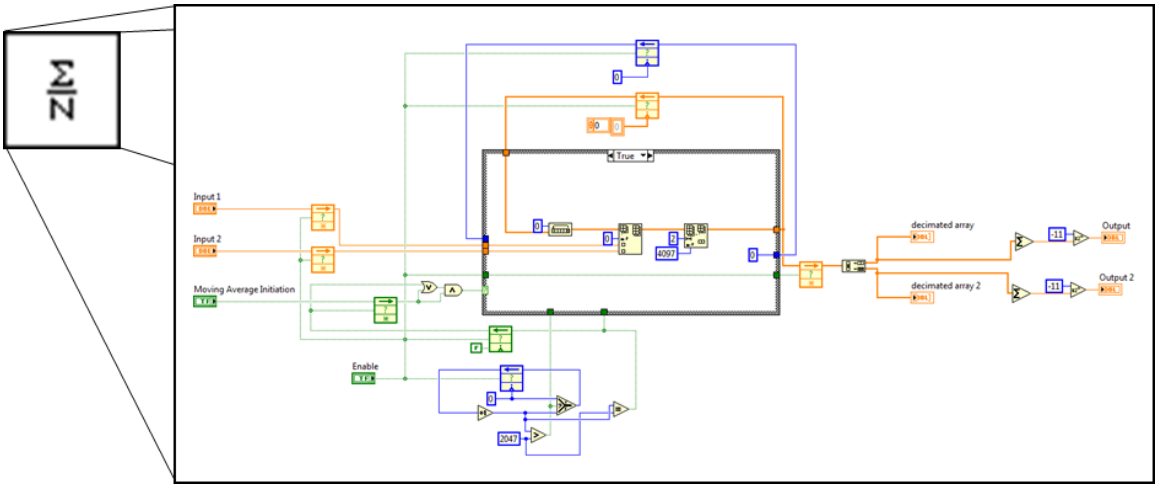
A.2.1.4 Sub VI – Virtual Stimulus Generation for Scale Factor Calibration



A.2.1.5 Sub VI – PI filter for Automatic Mode-Matching



A.2.1.6 Sub VI – Array-Based Moving-Average Filter (2048 Samples)



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